



# ENEE13020 *Digital Electronics*

## Term 1 - 2017

Profile information current as at 28/04/2024 03:41 am

All details in this unit profile for ENEE13020 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

## General Information

### Overview

You will be able to work in teams to model, analyse, design and verify digital electronic design projects. On satisfactory completion you will be able to discuss the application of digital electronics devices in information processing applications. In addition, you will be able to interpret functional requirements, research implementation options, analyse circuit performance, construct models for testing, verify system performance, and prepare project documents using symbols and terminologies that comply with Australian standards.

### Details

Career Level: *Undergraduate*

Unit Level: *Level 3*

Credit Points: 6

Student Contribution Band: 8

Fraction of Full-Time Student Load: 0.125

### Pre-requisites or Co-requisites

Prerequisites: (PHYS11185 Engineering Physics B OR ENAG11002 Energy and Electricity OR ENEG11009 Fundamentals of Energy and Electricity) AND (MATH11218 Applied Mathematics OR MATH11160 Technology Mathematics)

Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the [Assessment Policy and Procedure \(Higher Education Coursework\)](#).

### Offerings For Term 1 - 2017

- Bundaberg
- Cairns
- Distance
- Gladstone
- Mackay
- Rockhampton

### Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

### Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:

Click here to see your [Residential School Timetable](#).

### Website

[This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.](#)

## Class and Assessment Overview

### Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

### Class Timetable

#### [Regional Campuses](#)

Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

#### [Metropolitan Campuses](#)

Adelaide, Brisbane, Melbourne, Perth, Sydney

### Assessment Overview

#### 1. **Written Assessment**

Weighting: 20%

#### 2. **Written Assessment**

Weighting: 30%

#### 3. **Written Assessment**

Weighting: 20%

#### 4. **Practical and Written Assessment**

Weighting: 20%

#### 5. **Online Quiz(zes)**

Weighting: 10%

### Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the [University's Grades and Results Policy](#) for more details of interim results and final grades.

## CQUniversity Policies

**All University policies are available on the [CQUniversity Policy site](#).**

You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the [CQUniversity Policy site](#).

## Previous Student Feedback

### Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

#### Feedback from 'Have your say' survey

**Feedback**

Happy with the general flow of the course and the material was well structured.

**Recommendation**

The general flow of the course and the structured will be kept the same.

**Action**

The general flow of the course and the structured will be maintained.

#### Feedback from 'Have your say' survey

**Feedback**

The Design assignment was challenging but very interesting to undertake. The assignments and workbooks also related well to the course content.

**Recommendation**

The design and other assessment items will remain similar addressing the major sections learnt during the course.

**Action**

The design assignment and other assessment items will be maintained. However, streamlines of the tasks and improved marking criteria will be introduced and communicated to students within the tasks to further enhance learning and execution.

#### Feedback from 'Have your say' survey

**Feedback**

Multiple assessments to spread the load over.

**Recommendation**

The assessment items will be scheduled to submit at different times dividing the load over the term period.

**Action**

The assessment items will be scheduled to submit at different times dividing the load over the term period.

#### Feedback from 'Have your say' survey

**Feedback**

Multisim seems to be a poor choice of software, and made design assignment more focussed on software licencing issues than learning electronics

**Recommendation**

Multisim is an industry standard software used by most of the major companies and learning it will add the students an extra skill. The 50 number of component limit in the student version was solved by discussing with the software supplier and the new bundled version will have no component limits for students.

**Action**

Multisim is an industry standard software used by most of the major companies and learning it will enhance the students' skills. The 50 number of component limit in the student version was solved by discussing with the software supplier and the new bundled version will have no component limits for students.

## Unit Learning Outcomes

### On successful completion of this unit, you will be able to:

1. Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information.
2. Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices.
3. Interpret functional requirements, evaluate circuit options and conceive suitable system designs.
4. Verify operation of digital systems through software simulations and practical constructions of digital circuits.
5. Explain the various integrated circuit technologies and their future development trends.
6. Use appropriate electronic engineering terminologies and symbols that conform to the Australian Standards to prepare technical documentations for basic digital system designs and applications.
7. Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approach used to solve the problems.

The Learning Outcomes for this unit are linked with Engineers Australia's Stage 1 Competency Standard for Professional Engineers, Stage 1 Competency Standard for Engineering Technologists and Stage 1 Competency Standard for Engineering Associates.

## Alignment of Learning Outcomes, Assessment and Graduate Attributes



### Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Written Assessment - 20%	•	•				•	
2 - Written Assessment - 30%			•	•		•	•
3 - Written Assessment - 20%					•	•	
4 - Practical and Written Assessment - 20%	•	•		•		•	•
5 - Online Quiz(zes) - 10%	•	•			•		

### Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication	•		•	•	•	•	•
2 - Problem Solving	•	•	•	•			•
3 - Critical Thinking	•	•	•	•	•		•
4 - Information Literacy	•	•	•	•	•	•	•

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
5 - Team Work				•		•	•
6 - Information Technology Competence			•	•	•	•	•
7 - Cross Cultural Competence							•
8 - Ethical practice			•			•	•
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

### Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Written Assessment - 20%	•	•	•	•		•		•		
2 - Written Assessment - 30%	•	•	•	•	•	•		•		
3 - Written Assessment - 20%	•	•	•	•		•		•		
4 - Practical and Written Assessment - 20%	•	•	•	•	•	•		•		
5 - Online Quiz(zes) - 10%	•	•	•	•		•		•		

## Textbooks and Resources

### Textbooks

ENEE13020

#### Prescribed

##### Digital Fundamentals

Global Edition (11e) (15/12/2014)

Authors: Thomas L. Floyd

Pearson Higher Ed USA

U.S.A

ISBN: 9781292075983

Binding: Paperback

ENEE13020

#### Prescribed

##### NI Multisim Student Edition

Edition: 14.0 or later (2017)

Authors: National Instruments

National Instruments

USA

Binding: Paperback

#### Additional Textbook Information

**Textbook:** There is an electronic version of the prescribed textbook at a much more affordable price namely "Digital Fundamentals Global Edition VitalSource (11e)", ISBN 9781292075990. Please refer to the following webpage for ordering information <http://www.pearson.com.au/9781292075990>. However, paper copies are still available, if you prefer, through the CQUni Bookshop here: <http://bookshop.cqu.edu.au>

**Simulation software:** Students are required to use NI Multisim 14.0 to simulate electronic circuits for practicing of key learning concepts and doing the required assessment tasks in this course. This software is available on the campus wide network. For personal uses of the software at home, students can purchase a student edition of the software at a much reduced cost however this comes with a reduced functionality and limited capabilities in comparison to the full version of the software. The student edition of NI Multisim 14.0 can be ordered from the following webpage :<http://bookshop.cqu.edu.au>

[View textbooks at the CQUniversity Bookshop](#)

### IT Resources

**You will need access to the following IT resources:**

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Access to a computer with administrator rights where the latest version of Multisim software can be installed (needs Windows operating system)
- Access to a document scanner and a pdf converter
- Access to a suitable word processing software such as Microsoft word
- Access to NI Circuit Design Suite Software Package (Multisim version 14.0 or later)
- Headphones or speaker and a microphone

## Referencing Style

All submissions for this unit must use the referencing style: [Harvard \(author-date\)](#)

For further information, see the Assessment Tasks.

## Teaching Contacts

**Lam Bui** Unit Coordinator

[l.bui@cqu.edu.au](mailto:l.bui@cqu.edu.au)

## Schedule

### Week 1 - 06 Mar 2017

Module/Topic	Chapter	Events and Submissions/Topic
Introductory Concepts, Number Systems/Operations/Codes	Chapters 1 & 2	Online quizzes (worth 1%)

### Week 2 - 13 Mar 2017

Module/Topic	Chapter	Events and Submissions/Topic
Logic Gate	Chapter 3	

### Week 3 - 20 Mar 2017

Module/Topic	Chapter	Events and Submissions/Topic
Boolean Algebra and Logic Simplification	Chapter 4	Online quizzes (worth 2%)

### Week 4 - 27 Mar 2017

Module/Topic	Chapter	Events and Submissions/Topic
Combinational Logic Analysis	Chapter 5	

### Week 5 - 03 Apr 2017

Module/Topic	Chapter	Events and Submissions/Topic
Functions of Combinational Logic	Chapter 6	

### Vacation Week - 10 Apr 2017

Module/Topic	Chapter	Events and Submissions/Topic

### Week 6 - 17 Apr 2017

Module/Topic	Chapter	Events and Submissions/Topic
Latches, Flip-Flops and Timers	Chapter 7	Online quizzes (worth 2%) Residential School (Rockhampton) 22nd - 24th April 2017
		<b>Assessment 1</b> Due: Week 6 Monday (17 Apr 2017) 11:45 pm AEST

### Week 7 - 24 Apr 2017

Module/Topic	Chapter	Events and Submissions/Topic
Shift Registers	Chapter 8	

### Week 8 - 01 May 2017

Module/Topic	Chapter	Events and Submissions/Topic
Counters	Chapter 9	Laboratories 1 and 2 reports are due on Monday the 1st May 2017 at 23:45 pm Online quizzes (worth 2%)

### Week 9 - 08 May 2017

Module/Topic	Chapter	Events and Submissions/Topic
Programmable Logic	Chapter 10	

### Week 10 - 15 May 2017

Module/Topic	Chapter	Events and Submissions/Topic
Data Storage	Chapter 11	Online quizzes (worth 1%) <b>Design Assessment</b> Due: Week 10 Monday (15 May 2017) 11:45 pm AEST

## Week 11 - 22 May 2017

Module/Topic	Chapter	Events and Submissions/Topic
Signal Conversion and Processing	Chapter 12	Laboratories 3 and 4 reports are due on Monday the 22nd May 2017 at 23:45 pm Online quizzes (worth 1%)

## Week 12 - 29 May 2017

Module/Topic	Chapter	Events and Submissions/Topic
Integrated Circuit Technologies	Chapter 15	Online quizzes (worth 1%)

## Review/Exam Week - 05 Jun 2017

Module/Topic	Chapter	Events and Submissions/Topic
		<b>Assignment 2</b> Due: Review/Exam Week Monday (5 June 2017) 11:45 pm AEST

## Exam Week - 12 Jun 2017

Module/Topic	Chapter	Events and Submissions/Topic
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## Term Specific Information

It is strongly recommended that students attend the **first lecture** or view the **teaching arrangement slides** (available on **Moodle site**) where the essential information about the course will be provided including a) introducing the teaching team, b) outlining of teaching schedules, assessments and the due dates, c) prescribing of teaching resources (textbook, learning materials and software), d) residential school information (for mixed mode students only) and e) tips for a trouble-free term of studying this course!!!

## Assessment Tasks

### 1 Assessment 1

#### Assessment Type

Written Assessment

#### Task Description

This assessment is designed to test the knowledge relating to the learning outcomes for **Week 1 to Week 5**. Assignment 1 will be available from **Week 2** on the **Moodle site**. Please **complete all** the tasks and questions in the assignment.

#### Assessment Due Date

Week 6 Monday (17 Apr 2017) 11:45 pm AEST

Extension is only considered for a formal application received by 12:00 pm on the Friday prior to the deadline.

#### Return Date to Students

Monday (1 May 2017)

Marked assessments will be available for students to view a fortnight after the assessment due date.

#### Weighting

20%

#### Assessment Criteria

The instructions and mark allocation for each question will be shown on the assignment document. To achieve full mark, please read carefully, follow the instructions, and shows the full **step by step derivation** of your answers or solutions. Please refer to worked examples in the textbook to see what would be expected. If in doubt, please clarify with your local teaching staff.

#### Referencing Style

- [Harvard \(author-date\)](#)



## Submission

Online

### Submission Instructions

PDF document ONLY. NO HAND WRITTEN submission will be accepted!!! Please type and format your answers and solutions using a word processor and present your work in a professional manner.

### Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information.
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices.
- Use appropriate electronic engineering terminologies and symbols that conform to the Australian Standards to prepare technical documentations for basic digital system designs and applications.

### Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence
- Ethical practice

## 2 Design Assessment

### Assessment Type

Written Assessment

### Task Description

This is a design task and you are expected to carry out your own research and demonstrate the effective application of the knowledge learnt in this course up to the time of the assessment. This assessment will test your understanding of the materials from **Week 1** to **Week 9**. The design assessment will be available on the Moodle site from **Week 4**. There is no unique solution for the design, however you must justify all the design steps and component selections.

### Assessment Due Date

Week 10 Monday (15 May 2017) 11:45 pm AEST

Extension is only considered for a formal application received by 12:00 pm on the Friday prior to the deadline.

### Return Date to Students

Monday (29 May 2017)

Marked assessments will be available for students to view a fortnight after the assessment due date.

### Weighting

30%

### Minimum mark or grade

50%

### Assessment Criteria

The detailed assessment including description and mark allocation for each task is provided on the design assignment document. To achieve full mark, please read carefully, follow the instructions, and **shows the full step by step** derivation of your answers or solutions. The designed **MUST** be verified using **Multisim simulations**. There will be marks allocated for **technical writing** and therefore the design report must communicate the technical work clearly and succinctly and be prepared and laid out in a professional manner using a **word processor** (such as Microsoft word).

### Referencing Style

- [Harvard \(author-date\)](#)

## Submission

Online

### Submission Instructions

PDF document ONLY. NO HAND WRITTEN submission will be accepted!!! Please type and format your answers and solutions using a word processor and present your work in a professional manner.

### Learning Outcomes Assessed

- Interpret functional requirements, evaluate circuit options and conceive suitable system designs.
- Verify operation of digital systems through software simulations and practical constructions of digital circuits.

- Use appropriate electronic engineering terminologies and symbols that conform to the Australian Standards to prepare technical documentations for basic digital system designs and applications.
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approach used to solve the problems.

#### **Graduate Attributes**

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Team Work
- Information Technology Competence
- Ethical practice

### **3 Assignment 2**

#### **Assessment Type**

Written Assessment

#### **Task Description**

This is the second assignment and it is designed to assess the learning outcomes for **Week 5 to Week 12**. The assignment will be available on the Moodle site from **Week 4**.

#### **Assessment Due Date**

Review/Exam Week Monday (5 June 2017) 11:45 pm AEST

Extension is only considered for a formal application received by 12:00 pm on the Friday prior to the deadline.

#### **Return Date to Students**

Exam Week Friday (16 June 2017)

Marked assessments will be available for students to view a fortnight after the assessment due date.

#### **Weighting**

20%

#### **Assessment Criteria**

The instructions and mark allocation for each question will be shown on the assignment document. To achieve full mark, please read carefully, follow the instructions, and **shows the full step by step** derivation of your answers or solutions. Please refer to worked examples in the textbook to see what would be expected. If in doubt, please clarify with your local teaching staff.

#### **Referencing Style**

- [Harvard \(author-date\)](#)

#### **Submission**

Online

#### **Submission Instructions**

PDF document ONLY. NO HAND WRITTEN submission will be accepted!!! Please type and format your answers and solutions using a word processor and present your work in a professional manner.

#### **Learning Outcomes Assessed**

- Explain the various integrated circuit technologies and their future development trends.
- Use appropriate electronic engineering terminologies and symbols that conform to the Australian Standards to prepare technical documentations for basic digital system designs and applications.

#### **Graduate Attributes**

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence
- Ethical practice

### **4 Laboratories 1 to 4**

#### **Assessment Type**

Practical and Written Assessment

### Task Description

There are four laboratories in this course. **Laboratory 1** covers the materials of **Weeks 1-2**, **Laboratory 2** covers materials of **Weeks 3-5** and the last two laboratories (**Laboratory 3** and **Laboratory 4**) cover materials of **Week 6** and **Weeks 7-8** respectively. The step by step instructions to carry out these laboratories are provided in the laboratory documents. Students however require to perform tasks based on these guiding instructions, implement circuits, make measurements and record observations. There is also a personal reflection on the learning achieved from these laboratories.

The due dates for the laboratory reports are as following: Reports for **Laboratories 1 and 2** are due on **Monday 1st May 2017 at 23:45 pm** while the reports for **Laboratories 3 and 4** are due on **Monday 22nd May 2017 at 23:45 pm**.

### Assessment Due Date

Reports for Laboratories 1 and 2 are due on Monday 1st May 2017 at 23:45 pm and Reports for Laboratories 3 and 4 are due on Monday 22nd May 2017 at 23:45 pm.

### Return Date to Students

Marked assessments will be available for students to view a fortnight after the assessment due date.

### Weighting

20%

### Minimum mark or grade

50%

### Assessment Criteria

The instructions and mark allocation for each laboratory task are given the laboratory documents. To achieve full mark, please read carefully, follow the instructions, and shows the **full step by step derivation** of your answers or solutions. **Digital photographs** of your experiment setups or circuits must be included in the laboratory reports and please ensure that all essential components of your setup are clearly visible, labels could be used if necessary. If in doubt, please clarify with your local teaching staff.

### Referencing Style

- [Harvard \(author-date\)](#)

### Submission

Online

### Submission Instructions

PDF document ONLY. NO HAND WRITTEN submission will be accepted!!! Please type and format your answers and solutions using a word processor and present your work in a professional manner.

### Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information.
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices.
- Verify operation of digital systems through software simulations and practical constructions of digital circuits.
- Use appropriate electronic engineering terminologies and symbols that conform to the Australian Standards to prepare technical documentations for basic digital system designs and applications.
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approach used to solve the problems.

### Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Team Work
- Information Technology Competence
- Ethical practice

### 5 Online Quiz(zes)

### Assessment Type

Online Quiz(zes)

**Task Description**

Online quizzes will be available on the Moodle site prior to its given week and will **ONLY** be for **the weeks** that there is **no scheduled tutorial**. They provides excellent short-loop feedback to help students assessing their own understanding. **Online quizzes** will be marked but **DO NOT** base on the **number of correct answers, a full mark** will be awarded for just **simply attempt** and **complete the quizzes** by the end of the teaching term (**Monday the 5th June 2017** at 23:45 pm). For the detailed mark allocation for each online quizzes, please refer to the teaching schedule of this document.

**Number of Quizzes**

7

**Frequency of Quizzes**

Other

**Assessment Due Date**

Online quizzes are open throughout the term.

**Return Date to Students**

Online quizzes will be marked automatically

**Weighting**

10%

**Assessment Criteria**

Please follow the instructions that comes with the online quizzes. The majority of the questions will be of the multiple choice type. Please read the questions carefully and choose the **most correct** answer.

**Referencing Style**

- [Harvard \(author-date\)](#)

**Submission**

Online

**Submission Instructions**

You can attempt the quizzes as many times as you wish.

**Learning Outcomes Assessed**

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information.
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices.
- Explain the various integrated circuit technologies and their future development trends.

**Graduate Attributes**

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence
- Ethical practice

## Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the [Student Academic Integrity Policy and Procedure](#). This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

### What is a breach of academic integrity?

A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

### Why is academic integrity important?

A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

### Where can I get assistance?

For academic advice and guidance, the [Academic Learning Centre \(ALC\)](#) can support you in becoming confident in completing assessments with integrity and of high standard.

### What can you do to act with integrity?



#### Be Honest

If your assessment task is done by someone else, it would be dishonest of you to claim it as your own



#### Seek Help

If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)



#### Produce Original Work

Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem