ENEE13020 *Digital Electronics*

Term 1 - 2018

Profile information current as at 07/05/2024 06:50 am

All details in this unit profile for ENEE13020 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

General Information

Overview

Digital Electronics will provide you with the theoretical and practical knowledge of digital electronics devices in information processing applications. You will work in teams and individually to model, analyse, design and verify digital electronic design projects. Using software simulations and practical constructions of digital circuits you will verify operation of digital systems. You will develop the knowledge to analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices. You will learn to interpret functional requirements, research implementation options, construct models for testing and verify system performance. You will prepare project documents using symbols and terminologies that comply with Australian standards. Mixed mode students are required to attend a compulsory residential school and to pass the unit students must achieve at least 50% in the project assignment.

Details

Career Level: *Undergraduate*
Unit Level: *Level 3*
Credit Points: *6*
Student Contribution Band: *8*
Fraction of Full-Time Student Load: *0.125*

Pre-requisites or Co-requisites

Prerequisites: (PHYS11185 Engineering Physics B OR ENAG11002 Energy and Electricity OR ENEG11009 Fundamentals of Energy and Electricity) AND (MATH11218 Applied Mathematics OR MATH11160 Technology Mathematics)
Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the Assessment Policy and Procedure (Higher Education Coursework).

Offerings For Term 1 - 2018

- Bundaberg
- Cairns
- Gladstone
- Mackay
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:
Click here to see your Residential School Timetable.

Website

This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

Regional Campuses
Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

Metropolitan Campuses
Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Online Test**
Weighting: 15%
2. **Project (applied)**
Weighting: 40%
3. **Online Test**
Weighting: 15%
4. **Practical Assessment**
Weighting: 15%
5. **Practical Assessment**
Weighting: 15%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Policy for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the CQUniversity Policy site.
You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the CQUniversity Policy site.

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from "Have your say" Unit survey

Feedback

Students enjoyed the design assignment which required practicing of key learning concepts and creativity. Although it was challenging, it was achievable and resulted in deep learning of the taught materials.

Recommendation

The design assignment will be maintained as it provides a valuable learning opportunity to students.

Feedback from "Have your say" Unit survey

Feedback

Practical sessions were really enjoyable and eye opening!

Recommendation

Practical sessions are the major part of the unit and they will be maintained.

Feedback from "Have your say" Unit survey

Feedback

Materials were logically structured and well presented with very useful information throughout the term.

Recommendation

The overall flow and the content of the unit will be kept. Materials will be continuously revised and updated to enhance learning.

Feedback from "Have your say" Unit survey

Feedback

Assessments were very heavy with many assignment tasks and laboratory reports. Some of them were also too long for their contributions to the overall mark of the unit.

Recommendation

Assessments will be revised and consolidated to reduce both the number and the length. The overall mark will be redistributed among fewer assessment pieces to ensure fairer weighting.

Feedback from "Have your say" Unit survey

Feedback

Turnaround time for assessment marking was too long and more detailed feedback would be useful.

Recommendation

Consolidation of assessment tasks and introduction of an online test to replace one of the existing two assessments will be done to improve marking efficiency and therefore enable timely returns of mark and feedback to students. It is also planned to make use of marking template and make it available with the assessment task to improve marking transparency and provide more detailed feedback to students.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
2. Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
3. Interpret functional requirements, evaluate circuit options and conceive suitable system designs
4. Verify operation of digital systems though software simulations and practical constructions of digital circuits
5. Explain the various integrated circuit technologies and their future development trends
6. Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
7. Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

The Learning Outcomes for this unit are linked with Engineers Australia's Stage 1 Competency Standard for Professional Engineers, Stage 1 Competency Standard for Engineering Technologists, and Stage 1 Competency Standard for Engineering Associates.

Alignment of Learning Outcomes, Assessment and Graduate Attributes

— N/A Level | ● Introductory Level | ● Intermediate Level | ● Graduate Level | ○ Professional Level | ○ Advanced Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Online Test - 15%	●						
2 - Project (applied) - 40%		●	●			●	
3 - Online Test - 15%					●		
4 - Practical Assessment - 15%	●	●		●			●
5 - Practical Assessment - 15%				●			●

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication			●	●		●	●
2 - Problem Solving	●	●	●	●			●
3 - Critical Thinking	●	●	●	●	●		
4 - Information Literacy			●	●	●	●	●

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
5 - Team Work				•		•	•
6 - Information Technology Competence				•		•	•
7 - Cross Cultural Competence							•
8 - Ethical practice			•			•	•
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Online Test - 15%		•	•			•		•		
2 - Project (applied) - 40%	•	•	•	•		•		•		
3 - Online Test - 15%		•	•			•		•		
4 - Practical Assessment - 15%	•	•	•	•	•	•		•		
5 - Practical Assessment - 15%	•	•	•	•	•	•		•		

Textbooks and Resources

Textbooks

ENEE13020

Prescribed

Digital Fundamental
Eleventh Global Edition (2015)
Authors: Thomas L. Floyd
Pearson
USA
ISBN: 9781292075983
Binding: Other

Additional Textbook Information
There is an electronic version of the prescribed textbook at a much more affordable price namely "Digital Fundamentals Global Edition VitalSource (11e)", ISBN 9781292075990. Please refer to the following webpage for ordering information http://www.pearson.com.au/9781292075990. However, paper copies are still available, if you prefer, through the CQUni Bookshop here: http://bookshop.cqu.edu.au

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Microsft Office
- National Instruments, NI Multisim Education Edition, version 14 or later
- PC with Microsoft Windows as NI Multisim does not run non-windows platform

Referencing Style

All submissions for this unit must use the referencing style: Harvard (author-date)
For further information, see the Assessment Tasks.

Teaching Contacts

Lam Bui Unit Coordinator
l.bui@cqu.edu.au

Schedule

Week 1 - 05 Mar 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Overview of teaching arrangement • Introductory concepts	• Chapter 1 of textbook	• None

Week 2 - 12 Mar 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Number systems • Logic gates	• Chapter 2 and Chapter 3 of textbook	• None

Week 3 - 19 Mar 2018

Module/Topic	Chapter	Events and Submissions/Topic

• Boolean algebra and logic simplification	• Chapter 4	• Laboratory 1 part 1

Week 4 - 26 Mar 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Combinational logic analysis	• Chapter 5 of textbook	• Online test 1 opened (Friday)

Week 5 - 02 Apr 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Functions of combinational logic	• Chapter 6 of textbook	• Laboratory 1 part 2 • Online test 1 closed (Friday) **Online Test 1** Due: Week 5 Friday (6 Apr 2018) 11:59 pm AEST

Vacation Week - 09 Apr 2018

Module/Topic	Chapter	Events and Submissions/Topic
• No teaching	• Not applicable	• Residential school (April 12 - April 14)

Week 6 - 16 Apr 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Latches, flip-flops and timers	• Chapter 7 of textbook	• Laboratory 1 report due (Friday) **Laboratory 1 Report** Due: Week 6 Friday (20 Apr 2018) 11:59 pm AEST

Week 7 - 23 Apr 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Shift registers	• Chapter 8 of textbook	• Laboratory 2 part 1

Week 8 - 30 Apr 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Counters	• Chapter 9 of textbook	• None

Week 9 - 07 May 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Programmable logic	• Chapter 10 of textbook	• Laboratory 2 part 2 • Design project due (Friday) **Design Project** Due: Week 9 Friday (11 May 2018) 11:59 pm AEST

Week 10 - 14 May 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Data storage	• Chapter 11 of textbook	• Laboratory 2 report due (Friday) **Laboratory 2 Report** Due: Week 10 Friday (18 May 2018) 11:59 pm AEST

Week 11 - 21 May 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Signal conversion and processing	• Chapter 12 of textbook	• None

Week 12 - 28 May 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Integrated circuit technologies	• Chapter 15 of textbook	• Online test 2 opened (Friday)

Review/Exam Week - 04 Jun 2018

Module/Topic	Chapter	Events and Submissions/Topic

		• Online test 2 closed (Friday)
• No teaching	• Not applicable	**Online Test 2** Due: Review/Exam Week Friday (8 June 2018) 11:59 pm AEST
Exam Week - 11 Jun 2018		
Module/Topic	**Chapter**	**Events and Submissions/Topic**
• No examination	• Not applicable	• None

Assessment Tasks

1 Online Test 1

Assessment Type
Online Test

Task Description
Online test 1 is designed to assess student understanding and application of the materials covered between Week 1 and Week 4. This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform designs and calculations to arrive at the correct answer. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and thus it is advisable that you move on the next question if you are getting stuck at the current question. You only have ONE chance to complete the test. Good luck.

Assessment Due Date
Week 5 Friday (6 Apr 2018) 11:59 pm AEST
The test will be opened on Friday of Week 4 and closed on Friday of Week 5. It is important that the test MUST be completed within this period.

Return Date to Students
Week 8 Friday (4 May 2018)
Result of this test will be returned to students two weeks after the test closed

Weighting
15%

Assessment Criteria
Online test 1 aims to assess student understanding and application of the materials covered between Week 1 and Week 4 inclusively. In particular, the test will include questions relating to the following topics:

- Introductory concepts
- Binary arithmetic
- Compliments of binary numbers
- Number systems
- Codes and error correction
- Logic gates and programmable logic
- Boolean operations and algebra
- Standard forms of Boolean expressions
- Karnaugh map and expression minimization
- Combinational logic analysis and circuits
- Waveform operation

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 1 will be opened on Friday of Week 4 and closed on Friday of Week 5. It is important that this test MUST be completed within this period.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence
- Ethical practice

2 Design Project

Assessment Type
Project (applied)

Task Description
This project presents an opportunity for students to demonstrate their collective understanding of digital electronics and apply its principles and methods in the design of a practical real-life application. This project therefore requires students to integrate the learning and the materials covered between Week 1 and Week 8 inclusively. It therefore includes the following topics:

- Fundamental concepts
- Number systems
- Coding, decoding and codes conversions
- Combinational logic analysis
- Functions of combinational logic
- Digital memories and their operations
- Shift registers
- Digital Counters

Detailed descriptions of the project tasks are provided in the project information and the project report template. This project specifically requires students to conceive the system design based on the specified operational requirements of a real life application. Students will derive the relevant logic expressions and implement them as digital circuits in Multisim to demonstrate their correct operations. Students must also integrate these circuits together and show the correct operation of the entire system.
A complete project submission must contain ONLY TWO files: a single project report in PDF format and a single zipped file of a folder containing all relevant and necessary Multisim files that are executable by Multisim as they will be verified for the correct operations during the project marking.

Assessment Due Date
Week 9 Friday (11 May 2018) 11:59 pm AEST
A complete submission must contain only TWO files: a single PDF-file report and a single zipped file of a folder containing all relevant Multisim files in a single folder. This project MUST be submitted electronically via Moodle by the specified due time.

Return Date to Students
Week 11 Friday (25 May 2018)
Marked project reports will be returned to students two weeks after the project submission due date.

Weighting
40%

Minimum mark or grade
50%

Assessment Criteria

- Detailed of the project assessment criteria are provided in the project information document and project report template.
- Students must achieve a PASS (50% mark) on this project assessment to PASS this Unit.
- Students will be automatically failed if the Multisim files do not accompany the project submission. Please ensure that the Multisim files could be executed by the current version of Multisim (version 14) and they are not corrupted; a non-executable file is equal to non submitted file!!!

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete submission MUST and contains ONLY TWO files: a PDF project report and a zipped file containing all relevant Multisim files.

Learning Outcomes Assessed

- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence
- Ethical practice

3 Online Test 2

Assessment Type
Online Test

Task Description
Online test 2 is designed to assess student understanding and application of the materials covered between Week 9 and Week 12. This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform designs and calculations to arrive at the correct answer. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and thus it is advisable that you move on the next question if you are getting stuck at the current question. You only have ONE chance to complete the test. Good luck.

Assessment Due Date
Review/Exam Week Friday (8 June 2018) 11:59 pm AEST
Online test 2 will be opened on Friday of Week 12 and closed on Friday of Week 13 (Review/Exam Week). It is important that the test MUST be completed within this period.

Return Date to Students
Exam Week Friday (15 June 2018)
Result of this test is returned to students at the end of the Exam Week (Week 14).

Weighting
15%

Assessment Criteria
Online test 2 aims to assess student understanding and application of the materials covered between Week 9 and Week 12 inclusively. In particular, the test will include questions relating to the following topics:

- Programmable logic: architecture, operating modes, programming processes.
- Digital memories: architectures, operations, special types of memory, memory hierarchy
- Conversions between analog and digital signals: principles, methods, Nquist theorem, aliasing, quantisation error
- Electronic integrated technologies: MOSFET versus BJT, operational parameters, practical considerations

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 2 will be opened on Friday of Week 12 and closed on Friday of Week 13 (Review/Exam Week). It is important that this test MUST be completed within this period.

Learning Outcomes Assessed

- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence
- Ethical practice

4 Laboratory 1 Report

Assessment Type
Practical Assessment

Task Description
Laboratory 1 is designed to enhance student practical application of the materials covered between Week 1 and Week 5 inclusively. This laboratory aims to familiarize students with:

- Multisim as a circuit simulation tool for digital electronics
- Using breadboards as a circuit prototyping platform
- Digital integrated circuit (IC) chips
- Digital logic gates
- Logic expressions and their circuit implementations

Laboratory 1 comprises of two parts:

- Part 1 is conducted in Week 3 covering logic gates
- Part 2 is conducted in Week 5 covering logic expressions and circuits

Students are required to document the experimental results, discuss their findings and answer all questions provided in the laboratory instruction sheet and prepare the lab report using the provided laboratory template. Simulations of circuits will also be performed using Multisim as parts of the laboratory exercises.

Assessment Due Date
Week 6 Friday (20 Apr 2018) 11:59 pm AEST
A complete laboratory submission MUST consist of TWO files: a PDF lab report using the provided template and a single zipped file of a folder containing all relevant Multisim files in a single folder. Laboratory 1 MUST be submitted electronically via Moodle by the specified due time.

Return Date to Students
Week 8 Friday (4 May 2018)
Marked reports will be returned to students two weeks after the laboratory submission due date.

Weighting
15%

Assessment Criteria

- Details of assessment criteria and mark breakdown are given in the Laboratory 1 instruction sheet.
- The provided template MUST be used for preparing the laboratory report.
- The laboratory report must include all information and data to support your findings, discussions and answers of questions as each of these components will be allocated mark.
- There will be mark allocations for Multisim simulations. No mark will be awarded to non-submission or non-executable Multisim files. Please ensure that all relevant Multisim files are submitted and submit them as per submission instructions.
- Data, discussions and answers to questions must be complete and presented professionally as there will be a 10% mark awarded for technical completeness and presentation.
- Scanning of eligible hand-written texts and hand-drawn diagrams are acceptable, however it is strongly recommended that a suitable word processor is used to produce a high quality presentation.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete laboratory submission MUST consist of TWO files: a PDF lab report using the provided template and a single zipped file of a folder containing all relevant Multisim files in a single folder. Laboratory 1 MUST be submitted electronically via Moodle by the specified due time.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Team Work
- Information Technology Competence
- Ethical practice

5 Laboratory 2 Report

Assessment Type
Practical Assessment

Task Description
Laboratory 2 is designed to enhance student practical application of the materials covered between Week 6 and Week 8 inclusively. This laboratory aims to illustrate:

- Multisim as a tool for simulating sophisticated digital electronic circuits
- Operations of basic memory elements: latches and flip-flops
- Operations of a 555 timer
- Operations of shift registers
- Operations of digital counters

Laboratory 2 comprises of two parts:

- Part 1 is conducted in Week 7 covering latches, flip-flops and timers
- Part 2 is conducted in Week 9 covering shift registers, and counters

Students are required to document the experiment results, discuss their findings and answer all questions provided in the laboratory instruction sheet and prepare the lab report using the provided laboratory template.

Assessment Due Date
Week 10 Friday (18 May 2018) 11:59 pm AEST
A complete laboratory submission MUST consist of TWO files: a PDF lab report using the provided template and a single zipped file of a folder containing all relevant Multisim files in a single folder. Laboratory 2 MUST be submitted electronically via Moodle by the specified due time.

Return Date to Students
Week 12 Friday (1 June 2018)
Marked reports will be returned to students two weeks after the laboratory submission due date.

Weighting
15%

Assessment Criteria

- Details of assessment criteria and mark breakdown are given in the Laboratory 2 instruction sheet.
- The provided template MUST be used for preparing the laboratory report.
- The laboratory report must include all information and data to support your findings, discussions and answers of questions as each of these components will be allocated mark.
- There will be mark allocations for Multisim simulations. No mark will be awarded to non-submission or non-executable Multisim files. Please ensure that all relevant Multisim files are submitted and submit them as per submission instructions.

- Data, discussions and answers to questions must be complete and presented professionally as there will be a 10% mark awarded for technical completeness and presentation.
- Scanning of eligible hand-written texts and hand-drawn diagrams are acceptable, however it is strongly recommended that a suitable word processor is used to produce a high quality presentation.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete laboratory submission MUST consist of TWO files: a PDF lab report using the provided template and a single zipped file of a folder containing all relevant Multisim files in a single folder. Laboratory 2 MUST be submitted electronically via Moodle by the specified due time.

Learning Outcomes Assessed

- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Team Work
- Information Technology Competence
- Ethical practice

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the **Student Academic Integrity Policy and Procedure**. This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?
A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?
A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?
For academic advice and guidance, the Academic Learning Centre (ALC) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?

Be Honest
If your assessment task is done by someone else, it would be dishonest of you to claim it as your own

Seek Help
If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)

Produce Original Work
Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem