ENEE13020 *Digital Electronics*

Term 1 - 2019

Profile information current as at 02/05/2024 07:22 pm

General Information

Overview

Digital Electronics will provide you with the theoretical and the practical knowledge of digital electronics devices in information processing applications. You will work in teams and individually to model, analyse, design and verify digital electronic design projects. Using software simulations and practical constructions of digital circuits you will verify operation of digital systems. You will develop the knowledge to analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices. You will learn to interpret functional requirements, research implementation options, construct models for testing and verify system performance. You will prepare project documents using symbols and terminologies that comply with Australian standards. Mixed mode students are also required to attend a compulsory residential school and to pass this unit students must achieve at least 50% mark in the project assessment.

Details

Career Level: *Undergraduate*
Unit Level: *Level 3*
Credit Points: *6*
Student Contribution Band: *8*
Fraction of Full-Time Student Load: *0.125*

Pre-requisites or Co-requisites

Prerequisites: (PHYS11185 Engineering Physics B OR ENAG11002 Energy and Electricity OR ENEG11009 Fundamentals of Energy and Electricity) AND (MATH11218 Applied Mathematics OR MATH11160 Technology Mathematics)
Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the Assessment Policy and Procedure (Higher Education Coursework).

Offerings For Term 1 - 2019

- Bundaberg
- Cairns
- Gladstone
- Mackay
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:
Click here to see your Residential School Timetable.

Website

This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

Regional Campuses
Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

Metropolitan Campuses
Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Online Test**
Weighting: 15%
2. **Practical Assessment**
Weighting: 30%
3. **Project (applied)**
Weighting: 40%
4. **Online Test**
Weighting: 15%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Policy for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the CQUniversity Policy site.
You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the CQUniversity Policy site.

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from "Have your say" survey

Feedback
The design project was well received.

Recommendation
The design project will be maintained as it provides an opportunity for students to demonstrate their understanding and applications of the knowledge and concepts learned within this unit.

Feedback from "Have your say" survey

Feedback
A little more detail in the assessment requirements would be nicer, especially the design project.

Recommendation
A revision of the open-ended design project will be carried out to include more structure and instructions to ensure there is no ambiguity.

Feedback from "Have your say" survey

Feedback
Labs were quite well thought out and educational. They were interesting and the residential school helped quite a lot.

Recommendation
The laboratories and residential school are key learning activities. They will be maintained and made compulsory in this unit.

Feedback from "Have your say" survey

Feedback
Teaching teams are less equipped to support learning than the unit coordinator and lecturer.

Recommendation
Solutions to all tutorials and laboratories will be made available to the local teaching teams to allow them to support students better.

Feedback from "Have your say" survey

Feedback
The report was very time-consuming in its requirement for details.

Recommendation
The assessments will be reviewed and revised to ensure they are streamlined and there is no over-assessment of learning outcomes.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
2. Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
3. Interpret functional requirements, evaluate circuit options and conceive suitable system designs
4. Verify operation of digital systems though software simulations and practical constructions of digital circuits
5. Explain the various integrated circuit technologies and their future development trends
6. Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
7. Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

The Learning Outcomes for this unit are linked with Engineers Australia's Stage 1 Competency Standard for Professional Engineers, Stage 1 Competency Standard for Engineering Technologists, and Stage 1 Competency Standard for Engineering Associates.

Alignment of Learning Outcomes, Assessment and Graduate Attributes

— N/A Level · Introductory Level · Intermediate Level · Graduate Level ◦ Professional Level ◦ Advanced Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Online Test - 15%	•				•		
2 - Practical Assessment - 30%	•	•	•	•		•	•
3 - Project (applied) - 40%		•	•	•		•	•
4 - Online Test - 15%					•		

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication					•	•	•
2 - Problem Solving	•	•	•	•			
3 - Critical Thinking	•	•	•	•	•		
4 - Information Literacy			•		•	•	
5 - Team Work							•

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
6 - Information Technology Competence				•		•	•
7 - Cross Cultural Competence							
8 - Ethical practice							
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Online Test - 15%		•	•			•				
2 - Practical Assessment - 30%	•	•	•		•	•				
3 - Project (applied) - 40%	•	•	•	•		•				
4 - Online Test - 15%		•	•			•				

Textbooks and Resources

Textbooks

ENEE13020

Prescribed

Digital Fundamental
Eleventh Global Edition (2015)
Authors: Thomas L. Floyd
Pearson
USA
ISBN: 9781292075983
Binding: Paperback

Additional Textbook Information

Students are encouraged to order the prescribed textbook from the University bookshop here: http://bookshop.cqu.edu.au (search on the Unit code)

There is also an electronic version of the textbook at a reduced price called "Digital Fundamentals Global Edition VitalSource (11e)", ISBN 9781292075990. Please refer to the publisher's webpage for ordering information http://www.pearson.com.au/9781292075990

It is however recommended that a hard copy of the book is obtained for study and retained for future reference.

View textbooks at the CQUniversity Bookshop

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Microsft Office
- Zoom Conferencing (Webcam and Microphone)
- National Instruments, NI Multisim Education Edition, version 14 or later
- PC with Microsoft Windows as NI Multisim does not run non-windows platform

Referencing Style

All submissions for this unit must use the referencing style: Harvard (author-date)
For further information, see the Assessment Tasks.

Teaching Contacts

Lam Bui Unit Coordinator
l.bui@cqu.edu.au

Schedule

Week 1 - 11 Mar 2019

Module/Topic	Chapter	Events and Submissions/Topic

Overview of teaching arrangement Introductory concepts	Chapter 1 of textbook	None

Week 2 - 18 Mar 2019

Module/Topic	Chapter	Events and Submissions/Topic
Number systems Logic gates	Chapter 2 and Chapter 3 of textbook	None

Week 3 - 25 Mar 2019

Module/Topic	Chapter	Events and Submissions/Topic
Boolean algebra and logic simplification	Chapter 4 of textbook	None

Week 4 - 01 Apr 2019

Module/Topic	Chapter	Events and Submissions/Topic
Combinational logic analysis	Chapter 5 of textbook	None

Week 5 - 08 Apr 2019

Module/Topic	Chapter	Events and Submissions/Topic
Functions of combinational logic	Chapter 6 of textbook	Residential School (11-13 April 2019)

Vacation Week - 15 Apr 2019

Module/Topic	Chapter	Events and Submissions/Topic
No teaching	Not applicable	Online Test 1 opened (Friday)

Week 6 - 22 Apr 2019

Module/Topic	Chapter	Events and Submissions/Topic
Latches, flip-flops and timers	Chapter 7 of textbook	None **Online Test 1** Due: Week 6 Friday (26 Apr 2019) 12:59 pm AEST

Week 7 - 29 Apr 2019

Module/Topic	Chapter	Events and Submissions/Topic
Shift registers	Chapter 8 of textbook	None

Week 8 - 06 May 2019

Module/Topic	Chapter	Events and Submissions/Topic
Counters	Chapter 9 of textbook	None **Laboratory** Due: Week 8 Friday (10 May 2019) 12:59 pm AEST

Week 9 - 13 May 2019

Module/Topic	Chapter	Events and Submissions/Topic
Programmable logic	Chapter 10 of textbook	None

Week 10 - 20 May 2019

Module/Topic	Chapter	Events and Submissions/Topic
Data storage	Chapter 11 of textbook	None **Design Project** Due: Week 10 Friday (24 May 2019) 12:59 pm AEST

Week 11 - 27 May 2019

Module/Topic	Chapter	Events and Submissions/Topic
Signal conversion and processing	Chapter 12 of textbook	None

Week 12 - 03 Jun 2019

Module/Topic	Chapter	Events and Submissions/Topic
Integrated circuit technologies	Chapter 15 of textbook	Online Test 2 opened (Friday)

Review/Exam Week - 10 Jun 2019

Module/Topic	Chapter	Events and Submissions/Topic
		None
No teaching	Not applicable	**Online Test 2** Due: Review/Exam Week Friday (14 June 2019) 12:59 pm AEST

Exam Week - 17 Jun 2019

Module/Topic	Chapter	Events and Submissions/Topic
No examination	Not applicable	None

Term Specific Information

Residential school is compulsory for mixed mode students. If student cannot attend the residential school, he/she must arrange with the Unit Coordinator to attend the laboratories with on-campus students at one of the campus locations where the unit is running at the start of term (.i.e prior to Week 3 of term).

Assessment Tasks

1 Online Test 1

Assessment Type
Online Test

Task Description
Online Test 1 is designed to assess student understanding and application of the materials covered between Week 1 and Week 4. Particularly, the test will include questions relating to the following topics:

- Introductory concepts
- Binary arithmetic
- Compliments of binary numbers
- Number systems
- Codes and error correction
- Logic gates and programmable logic
- Boolean operations and algebra
- Standard forms of Boolean expressions
- Karnaugh map and expression minimization
- Combinational logic analysis and circuits
- Waveform operation

This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform designs and calculations to arrive at the correct answers. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and therefore it is advisable that you move on the next question if you are getting stuck at the current question. You have only ONE chance to complete the test. Good luck.

Assessment Due Date
Week 6 Friday (26 Apr 2019) 12:59 pm AEST
The test will be opened on Friday of Week 5 and closed on Friday of Week 6. It is important that the test MUST be completed within this period.

Return Date to Students
Week 8 Friday (10 May 2019)
Result of assessment will be returned to students within two weeks after the due date.

Weighting
15%

Assessment Criteria
For each question, student must choose the right most answer. Only correct answer chosen results in an award of a full mark for that question. Wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online Test 1 will be opened on Friday of Week 5 and closed on Friday of Week 6. It is important that this test MUST be completed within this period.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

2 Laboratory

Assessment Type
Practical Assessment

Task Description
Laboratory comprises of two parts. Part 1 is designed to enhance student practical application of the materials covered between Week 1 and Week 5 inclusively and aims to familiarize students with:

- Multisim as a circuit simulation tool for digital electronics
- Using breadboards as a circuit prototyping platform
- Digital integrated circuit (IC) chips
- Digital logic gates
- Logic expressions and their circuit implementations

Part 2 is designed to enhance student practical application of the materials covered between Week 6 and Week 8 inclusively and aims to illustrate:

- Multisim as a tool for simulating sophisticated digital electronic circuits
- Operations of basic memory elements: latches and flip-flops
- Operations of a 555 timer
- Operations of shift registers
- Operations of digital counters

Students are required to document the experimental results, discuss their findings and answer all questions provided in the laboratory instruction sheet and prepare the lab report using the provided report template. Simulations of circuits will also be performed using Multisim as parts of the laboratory exercises.

Assessment Due Date
Week 8 Friday (10 May 2019) 12:59 pm AEST
A complete laboratory submission MUST consist of TWO files: 1) a PDF lab report and 2) a single zipped file containing all relevant Multisim files in a single folder. Laboratory MUST be submitted electronically via the Moodle link by the due date.

Return Date to Students
Week 10 Monday (20 May 2019)
Marked reports will be returned to students within two weeks after the laboratory submission due.

Weighting
30%

Minimum mark or grade
50%

Assessment Criteria
The provided template MUST be used for preparing the laboratory report.

- The details of assessment criteria and mark allocation are given in the Laboratory instruction sheet.
- The laboratory report must include all information and data to support your findings, discussions and answers of questions as each of these components will be marked.
- There will be mark allocations for Multisim simulations. No mark will be awarded to non-submission or nonexecutable Multisim files. Please ensure that all relevant Multisim files are submitted and submit them as per submission instructions.
- Data, discussions and answers to questions must be complete and presented professionally as there will be some marks awarded for technical completeness and presentation.
- Scanning of eligible hand-written texts and hand-drawn diagrams are acceptable, however it is strongly recommended that a suitable word processor is used to produce a professional presentation.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete laboratory submission MUST consist of TWO files: 1) a PDF lab report and 2) a single zipped file containing all relevant Multisim files in a single folder. Laboratory MUST be submitted electronically via the Moodle link by the due date.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Team Work
- Information Technology Competence

3 Design Project

Assessment Type
Project (applied)

Task Description
This project presents an opportunity for students to demonstrate their collective understanding of digital electronics and apply its principles and methods in the design of a practical real-life application. This project therefore requires students to integrate the learning and the materials covered between Week 1 and Week 8 inclusively. It therefore includes the following topics:

- Fundamental concepts
- Number systems
- Coding, decoding and codes conversions
- Combinational logic analysis
- Functions of combinational logic
- Digital memories and their operations

- Shift registers
- Digital Counters

Detailed descriptions of the project tasks are provided in the project information and the project report template. This project specifically requires students to conceive the system design based on the specified operational requirements of a real life application. Students will derive the relevant logic expressions and implement them as digital circuits in Multisim to demonstrate their correct operations. Students must also integrate these circuit modules together and show the correct operation of the entire system.
A complete project submission must contain ONLY TWO files: a single project report in PDF format and a single zipped file of a folder containing all relevant and necessary Multisim files that are executable by Multisim as they will be verified for the correct operations during the project marking.

Assessment Due Date
Week 10 Friday (24 May 2019) 12:59 pm AEST
A complete submission must contain only TWO files: 1) a single PDF-file report and 2) a single zipped file of a folder containing all relevant Multisim files in a single folder. This project MUST be submitted electronically via Moodle by the specified due time.

Return Date to Students
Week 12 Friday (7 June 2019)
Marked project reports will be returned to students within two weeks after the project submission due date.

Weighting
40%

Minimum mark or grade
50%

Assessment Criteria

- The detailed assessment criteria are provided in the project information document and the project report template.
- Project report MUST follow the the provided report template.
- Students must achieve a PASS grade (50% mark) on the project to PASS this Unit.
- Students will be automatically failed if the Multisim files do not accompany the project submission. Please ensure that the Multisim files could be executed by the current version of Multisim (version 14) and they are not
- corrupted as a non-executable file is equal to non submitted file!

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete submission MUST and contains ONLY TWO files: 1) a PDF project report and 2) a zipped file containing all relevant Multisim files.

Learning Outcomes Assessed

- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence

4 Online Test 2

Assessment Type
Online Test

Task Description
Online test 2 is designed to assess student understanding and application of the materials covered between Week 9 and Week 12. Particularly, the test will include questions relating to the following topics:

- Programmable logic: architecture, operating modes, programming processes.
- Digital memories: architectures, operations, special types of memory, memory hierarchy
- Conversions between analog and digital signals: principles, methods, Nquist theorem, aliasing, quantisation error
- Electronic integrated technologies: MOSFET versus BJT, operational parameters, and practical considerations

This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform designs and calculations to arrive at the correct answers. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and therefore it is advisable that you move on the next question if you are getting stuck at the current question. You have only ONE chance to complete the test. Good luck.

Assessment Due Date
Review/Exam Week Friday (14 June 2019) 12:59 pm AEST
Online test 2 will be opened on Friday of Week 12 and closed on Friday of Week 13 (Review/Exam Week). It is important

Return Date to Students
Exam Week Friday (21 June 2019)
Test results are to be returned to students within two weeks of the test completion.

Weighting
15%

Assessment Criteria
For each question, student must choose the right most answer. Only correct answer chosen results in an award of a full mark for that question. Wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online Test 2 will be opened on Friday of Week 12 and closed on Friday of Week 13 (Review/Exam Week). It is important that the test MUST be completed within this period.

Learning Outcomes Assessed

- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the **Student Academic Integrity Policy and Procedure**. This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?
A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?
A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?
For academic advice and guidance, the Academic Learning Centre (ALC) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?

Be Honest
If your assessment task is done by someone else, it would be dishonest of you to claim it as your own

Seek Help
If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)

Produce Original Work
Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem