ENEE13020 *Digital Electronics*
Term 1 - 2020

Profile information current as at 29/04/2024 06:30 am

All details in this unit profile for ENEE13020 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

Corrections

Unit Profile Correction added on 17-04-20

All teaching activities are shifted online via recorded videos of lectures and tutorials and interactive Zoom sessions instead of classroom based activities. Lab kits are sent to students' homes and students do the lab at home with assistance from lecturer via a Zoom based demonstration session. There is no change to the unit's assessments as they are already project based and online tests.

General Information

Overview

Digital Electronics will provide you with the theoretical and the practical knowledge of digital electronics devices in information processing applications. You will work in teams and individually to model, analyse, design and verify digital electronic design projects. Using software simulations and practical constructions of digital circuits you will verify operation of digital systems. You will develop the knowledge to analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices. You will learn to interpret functional requirements, research implementation options, construct models for testing and verify system performance. You will prepare project documents using symbols and terminologies that comply with Australian standards. Mixed mode students are also required to attend a compulsory residential school and to pass this unit students must achieve at least 50% mark in the project assessment.

Details

Career Level: *Undergraduate*
Unit Level: *Level 3*
Credit Points: *6*
Student Contribution Band: *8*
Fraction of Full-Time Student Load: *0.125*

Pre-requisites or Co-requisites

Prerequisites: (PHYS11185 Engineering Physics B OR ENAG11002 Energy and Electricity OR ENEG11009 Fundamentals of Energy and Electricity) AND (MATH11218 Applied Mathematics OR MATH11160 Technology Mathematics)
Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the Assessment Policy and Procedure (Higher Education Coursework).

Offerings For Term 1 - 2020

- Bundaberg
- Cairns
- Gladstone
- Mackay
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:
Click here to see your Residential School Timetable.

Website

This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

Regional Campuses
Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

Metropolitan Campuses
Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Online Test**
Weighting: 15%
2. **Practical Assessment**
Weighting: 30%
3. **Project (applied)**
Weighting: 40%
4. **Online Test**
Weighting: 15%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Policy for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the CQUniversity Policy site.
You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the CQUniversity Policy site.

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from "Have your say" survey

Feedback
The online tests were really good. They helped to reinforce and consolidate learning materials.

Recommendation
The online test is an integral part of the teaching and learning of this unit as it encourages students to review the materials taught and provides prompt feedback to students about their learning and understanding. Having early feedback also improves student experience and satisfaction with this unit.

Feedback from "Have your say" survey

Feedback
The design project was very tough but a rewarding assessment piece that really solidified the entire unit content.

Recommendation
The design project provides an important learning opportunity for students within this unit and therefore it will be maintained and continuously be improved. However, the current project has been perceived to be a bit over challenging for most students. This consequently affects unit satisfaction. A revision of the project will be carried out to align the project's requirements with the student level to improve student's experiences.

Feedback from "Have your say" survey

Feedback
The scope of the design project was a bit too open to interpretation and thus it would be more helpful if the design requirements can be specified more specifically.

Recommendation
The openness of the project scope has created difficulties for many students who are not familiar and/or have little experience with research. This, unfortunately, has a negative impact on the unit's satisfaction for these students. To improve student experience with the project, the design scope will be narrowed down to reduce its openness and more explanation and scaffolding guidance toward the project end goals will be provided to assist students with this task.

Feedback from "Have your say" survey

Feedback
Residential school and the laboratory exercises were very helpful to help students learn the key concepts introduced in the lecture and assist students with the completion of the assessment tasks.

Recommendation
The residential school and laboratory will be maintained and its content and delivery will continue to be improved, especially providing more guidance on the practical aspects of the laboratory.

Feedback from "Have your say" survey

Feedback
Tutorials were well designed to support learning by using step by step progression from simple to complex problems.

Recommendation
Tutorials will continue to be provided as supplementary learning support for the lectures.

Feedback from "Have your say" survey

Feedback
It would be helpful if the assessment due dates were on the weekend rather than on Friday as it had been difficult to meet these deadlines due to work commitments.

Recommendation
Submission due dates of the assessments will be revised and where possible inclusion of the weekend will be considered and accommodated. It is anticipated that these small changes of setting assessment due dates would also improve overall satisfaction with the unit.

Feedback from "Have your say" survey

Feedback
Better support for learning NI Multisim would be beneficial to students who had little experiences with this simulation package.

Recommendation
More guidance for the learning of the Multisim software will be provided to students in the early few weeks of term to get students up to speed with using the simulation software. This will help students do better with the design project and thus improves unit satisfaction.

Feedback from Student direct feedback to Unit Coordinator

Feedback
The assessments require independent research to be carried out by students which demand much time to complete.

Recommendation
Assessment tasks, especially the Design Project's requirements will be revised to make sure that it is better aligned with the lecture contents to reduce the research component involved. Since it is necessary to engage students, especially the high achievers in some research work, a small research component will be retained within the project to enable these students to demonstrate a higher level of achievement. This will also improve the unit outcome and satisfaction.

Feedback from Unit Coordinator's observation

Feedback
The assessment instructions and guidance could be more comprehensive.

Recommendation
Additional guidelines and instructions on the assessments will be communicated to students prior to the assessment tasks to improve student understanding of what is required and expected for the tasks and thus improve their satisfaction with the assessments.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
2. Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
3. Interpret functional requirements, evaluate circuit options and conceive suitable system designs
4. Verify operation of digital systems though software simulations and practical constructions of digital circuits
5. Explain the various integrated circuit technologies and their future development trends
6. Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
7. Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

The Learning Outcomes for this unit are linked with Engineers Australia's Stage 1 Competency Standard for Professional Engineers, Stage 1 Competency Standard for Engineering Technologists, and Stage 1 Competency Standard for Engineering Associates.

Alignment of Learning Outcomes, Assessment and Graduate Attributes

— N/A Level ◦ Introductory Level • Intermediate Level • Graduate Level ◦ Professional Level ◦ Advanced Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Online Test - 15%	•				•		
2 - Practical Assessment - 30%	•	•	•	•		•	•
3 - Project (applied) - 40%		•	•	•		•	•
4 - Online Test - 15%					•		

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication					•	•	•
2 - Problem Solving	•	•	•	•			
3 - Critical Thinking	•	•	•	•	•		
4 - Information Literacy			•		•	•	
5 - Team Work							•
6 - Information Technology Competence				•		•	•
7 - Cross Cultural Competence							
8 - Ethical practice							
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Online Test - 15%		•	•			•				
2 - Practical Assessment - 30%	•	•	•		•	•				
3 - Project (applied) - 40%	•	•	•	•		•				
4 - Online Test - 15%		•	•			•				

Textbooks and Resources

Textbooks

ENEE13020

Prescribed

Digital Fundamental
Eleventh Global Edition (2015)
Authors: Thomas L. Floyd
Pearson
Harlow , Essex , England
ISBN: 9781292075983
Binding: Paperback

Additional Textbook Information
There is also an electronic version of the textbook at a reduced price called "Digital Fundamentals Global Edition VitalSource (11e)", ISBN 9781292075990. Please refer to the publisher's webpage for ordering information http://www.pearson.com.au/9781292075990
However, paper copies can still be purchased from the CQUni Bookshop here: http://bookshop.cqu.edu.au (search on the Unit code)

View textbooks at the CQUniversity Bookshop

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Microsft Office
- Zoom Conferencing (Webcam and Microphone)
- National Instruments, NI Multisim Education Edition, version 14 or later
- PC with Microsoft Windows as NI Multisim does not run non-windows platform

Referencing Style

All submissions for this unit must use the referencing style: Harvard (author-date)
For further information, see the Assessment Tasks.

Teaching Contacts

Lam Bui Unit Coordinator
l.bui@cqu.edu.au

Schedule

Week 1 - 09 Mar 2020

Module/Topic	Chapter	Events and Submissions/Topic
Overview of teaching arrangement Introductory concepts	Chapter 1 of textbook	None

Week 2 - 16 Mar 2020

Module/Topic	Chapter	Events and Submissions/Topic
Number systems and Logic gates	Chapters 2 and 3 of textbook	None

Week 3 - 23 Mar 2020

Module/Topic	Chapter	Events and Submissions/Topic
Boolean algebra and Logic simplification	Chapter 4 of textbook	None

Week 4 - 30 Mar 2020

Module/Topic	Chapter	Events and Submissions/Topic
Combinational logic analysis	Chapter 5 of textbook	None

Week 5 - 06 Apr 2020

Module/Topic	Chapter	Events and Submissions/Topic
Functions of combinational logic	Chapter 6 of textbook	None

Vacation Week - 13 Apr 2020

Module/Topic	Chapter	Events and Submissions/Topic
No teaching	Not applicable	Online test 1 opened (Friday)

Week 6 - 20 Apr 2020

Module/Topic	Chapter	Events and Submissions/Topic
Latches, flip-flops and timers	Chapter 7 of textbook	

Week 7 - 27 Apr 2020

Module/Topic	Chapter	Events and Submissions/Topic
Shift registers	Chapter 8 of textbook	Residential School (30 April - 2 May 2020) **Online Test 1** Due: Week 7 Monday (27 Apr 2020) 11:59 pm AEST

Week 8 - 04 May 2020

Module/Topic	Chapter	Events and Submissions/Topic
Counters	Chapter 9 of textbook	None

Week 9 - 11 May 2020

Module/Topic	Chapter	Events and Submissions/Topic
Programmable logic	Chapter 10 of textbook	None **Laboratory Report** Due: Week 9 Monday (11 May 2020) 11:59 pm AEST

Week 10 - 18 May 2020

Module/Topic	Chapter	Events and Submissions/Topic
Data storage	Chapter 11 of textbook	None

Week 11 - 25 May 2020

Module/Topic	Chapter	Events and Submissions/Topic
Signal conversion and processing	Chapter 12 of textbook	None **Design Project** Due: Week 11 Monday (25 May 2020) 11:59 pm AEST

Week 12 - 01 Jun 2020

Module/Topic	Chapter	Events and Submissions/Topic
Integrated circuit technologies	Chapter 15 of textbook	Online test 2 opened (Friday)

Review/Exam Week - 08 Jun 2020

Module/Topic	Chapter	Events and Submissions/Topic
No teaching	Not applicable	None

Exam Week - 15 Jun 2020		
Module/Topic	**Chapter**	**Events and Submissions/Topic**
		None
No examination	Not applicable	**Online Test 2** Due: Exam Week Monday (15 June 2020) 11:59 pm AEST

Term Specific Information

Residential school is a compulsory learning activity for mixed mode students. If a student cannot attend the residential school for a reason outside of his or her control, he or she must arrange with the Unit Coordinator by the end of Week 3 of term to attend the laboratories with the on-campus students at one of the campus locations where the unit are offering.

Assessment Tasks

1 Online Test 1

Assessment Type
Online Test

Task Description
Online test 1 is designed to assess student understanding and application of the materials covered between Week 1 and Week 5. Particularly, the test will include questions relating to the topics of:

- Introductory concepts
- Binary arithmetic
- Compliments of binary numbers
- Number systems
- Codes and error correction
- Logic gates and programmable logic
- Boolean operations and algebra
- Standard forms of Boolean expressions
- Karnaugh map and expression minimization
- Combinational logic analysis and circuits
- Waveform operation
- Functions of combinational logic

The test is multiple choice question and timed. Some of the questions may require students to perform a design and calculations to arrive at the correct answer. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test automatically closes when the test time elapses and therefore it is advisable that you move quickly to the next question if getting stuck. Please be aware that you have only ONE chance to complete the test.

Assessment Due Date
Week 7 Monday (27 Apr 2020) 11:59 pm AEST
The test opens on Friday of Week 5 and closes on Monday of Week 7. It is important to complete the test within this period since after closing the test cannot be reopened.

Return Date to Students
Week 9 Monday (11 May 2020)
Test results are often returned to students within two weeks after the test closes.

Weighting
15%

Assessment Criteria
For each question, student must choose the most correct answer. Only correct answer results in the award of a full mark. A wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 1 opens on Friday of Week 5 and closes on Monday of Week 7. It is important to complete the test within this period as after closing the test cannot be reopened.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

2 Laboratory Report

Assessment Type
Practical Assessment

Task Description
Laboratory comprises of two parts. Part 1 is designed to enhance student practical application of the materials covered between Week 1 and Week 5 inclusively. The laboratory part 1 aims to familiarize students with:

- Multisim as a circuit simulation tool for digital electronics
- Using breadboards as a circuit prototyping platform
- Digital integrated circuit (IC) chips
- Digital logic gates
- Logic expressions and their circuit implementations

Part 2 is designed to enhance student practical application of the materials covered between Week 6 and Week 8 inclusively. The laboratory exercises aim to illustrate

- Multisim as a tool for simulating sophisticated digital electronic circuits
- Operations of basic memory elements: latches and flip-flops
- Operations of a 555 timer
- Operations of shift registers
- Operations of digital counters

Students are required to document the laboratory results, discuss their findings in detailed and answer all questions provided in the laboratory instruction sheet. The lab report must be completed using the provided laboratory template. Simulations of circuits must also be performed using Multisim as instructed in the laboratory instructions.

Assessment Due Date
Week 9 Monday (11 May 2020) 11:59 pm AEST
A complete laboratory submission MUST consist of TWO and only two files: 1) a lab report in pdf format and 2) a single zipped file containing all relevant Multisim files used for the lab report. Laboratory files MUST be submitted electronically via Moodle by the deadline

Return Date to Students
Week 11 Monday (25 May 2020)
Marked reports often return to students within two weeks of submission deadline.

Weighting
30%

Minimum mark or grade
50%

Assessment Criteria
The provided laboratory template MUST be used for preparing the laboratory report.

- The details of assessment criteria and mark allocation are given as in the Laboratory instruction sheet.
- The laboratory report must include all information and data to support findings. Discussions and answers of questions must be complete as they will be marked.
- There will be marks allocations for Multisim simulations. No mark is awarded for missing or not-working Multisim files. Please ensure that all relevant Multisim files are submitted as per the submission instructions.

- Data, discussions and answers to questions must be consistent and presented professionally as marks are reserved and awarded for technical rigor and completeness.
- Scanning of hand-written texts or hand-drawn diagrams are acceptable but they must be legible. It is strongly recommended that a suitable drawing software are used to produce a professionally looking report.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete laboratory submission MUST consist of TWO and only two files: 1) a lab report in pdf format and 2) a single zipped file containing all relevant Multisim files used for the lab report. Laboratory files MUST be submitted electronically via Moodle by the deadline

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Team Work
- Information Technology Competence

3 Design Project

Assessment Type
Project (applied)

Task Description
This project presents an opportunity for students to demonstrate their collective understanding of digital electronics and apply its principles and methods in the design of practical real-life applications. This project therefore requires students to integrate the learning and the materials covered between Week 1 and Week 8 inclusively. The project requires knowledge of the following topics:

- Fundamental concepts
- Number systems
- Coding, decoding and codes conversions
- Combinational logic analysis
- Functions of combinational logic
- Digital memories and their operations
- Shift registers
- Digital Counters

A detailed description of the project is provided in the project information document and the project reporting template. This project specifically requires students to conceive the system design based on the specified operational requirements of a real life application. The project must be designed in a modular form where students derive the relevant logic expression for each module, implement the modules one by one and demonstrate their correct operation using Multisim simulations. Students also require to integrate the modules together to create a complete working system.
A complete project submission must contain ONLY TWO files: 1) a single project report in a PDF format and 2) a single zipped file containing all relevant and necessary Multisim file implementation of the project that are executable using

Multisim. The Multisim implementation of the project will be executed to verify for correct operations during project marking.

Assessment Due Date
Week 11 Monday (25 May 2020) 11:59 pm AEST
A complete submission must contain of TWO only two files: 1) a single report file in pdf format and 2) a single zipped file of all relevant Multisim implementations/simulations of the project. The project files MUST be submitted electronically via Moodle by the deadline

Return Date to Students

Project mark will not be available to students until after the unit grades are finalised

Weighting
40%

Minimum mark or grade
50%

Assessment Criteria

- The detailed assessment criteria are provided in the project information document and the project reporting template.
- The project report MUST be completed using the the provided reporting template.
- Students must achieve at least 50% mark for the project to PASS this unit.
- No mark is awarded for parts of report with missing or not working Multisim files. Please also ensure that the submitted Multisim files are executable by the current version of Multisim (version 14).

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete submission MUST and contains ONLY TWO files: 1) a PDF project report and 2) a zipped file containing all relevant Multisim files.

Learning Outcomes Assessed

- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence

4 Online Test 2

Assessment Type
Online Test

Task Description
Online test 2 is designed to assess student understanding and application of the materials covered between Week 9 and Week 12. Particularly, the test will include questions relating to the following topics:

- Programmable logic: architecture, operating modes, programming processes.

- Digital memories: architectures, operations, special types of memory, memory hierarchy
- Conversions between analog and digital signals: principles, methods, Nquist theorem, aliasing, quantisation error
- Electronic integrated technologies: MOSFET versus BJT, operational parameters, and practical considerations

This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform a design and calculations to arrive at the correct answers. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and therefore it is advisable that you move quickly to the next question if you are getting stuck at the current question. Please be aware that you have only ONE chance to complete the test.

Assessment Due Date
Exam Week Monday (15 June 2020) 11:59 pm AEST
Online test 2 will be opened on Friday of Week 12 and closed on Monday of Week 14 (Exam Week). It is important to complete the test within this period as the test cannot be reopened after closing

Return Date to Students
Exam Week Friday (19 June 2020)
Test results will be released to students within two weeks after closing.

Weighting
15%

Assessment Criteria
For each question, student must choose the most correct answer. Only correct answer results in the award of a full mark. A wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 2 will be opened on Friday of Week 12 and closed on Monday of Week 14 (Exam Week). It is important to complete the test within this period as the test cannot be reopened after closing

Learning Outcomes Assessed

- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the **Student Academic Integrity Policy and Procedure**. This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?
A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?
A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?
For academic advice and guidance, the Academic Learning Centre (ALC) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?

Be Honest
If your assessment task is done by someone else, it would be dishonest of you to claim it as your own

Seek Help
If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)

Produce Original Work
Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem