ENEE13020 *Digital Electronics*

Term 1 - 2021

Profile information current as at 04/05/2024 11:22 am

General Information

Overview

Digital Electronics will provide you with the theoretical and the practical knowledge of digital electronics devices in information processing applications. You will work in teams and individually to model, analyse, design and verify digital electronic design projects. Using software simulations and practical constructions of digital circuits you will verify operation of digital systems. You will develop the knowledge to analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices. You will learn to interpret functional requirements, research implementation options, construct models for testing and verify system performance. You will prepare project documents using symbols and terminologies that comply with Australian standards. Mixed mode students are also required to attend a compulsory residential school and to pass this unit students must achieve at least 50% mark in the project assessment.

Details

Career Level: *Undergraduate*
Unit Level: *Level 3*
Credit Points: *6*
Student Contribution Band: *8*
Fraction of Full-Time Student Load: *0.125*

Pre-requisites or Co-requisites

Prerequisites: (PHYS11185 Engineering Physics B OR ENAG11002 Energy and Electricity OR ENEG11009 Fundamentals of Energy and Electricity) AND (MATH11218 Applied Mathematics OR MATH11160 Technology Mathematics)
Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the Assessment Policy and Procedure (Higher Education Coursework).

Offerings For Term 1 - 2021

- Bundaberg
- Cairns
- Gladstone
- Mackay
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:
Click here to see your Residential School Timetable.

Website

This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

Regional Campuses
Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

Metropolitan Campuses
Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Online Test**
Weighting: 15%
2. **Practical Assessment**
Weighting: 30%
3. **Project (applied)**
Weighting: 40%
4. **Online Test**
Weighting: 15%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Policy for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the CQUniversity Policy site.
You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the CQUniversity Policy site.

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from Unit's survey

Feedback
Clear communications from the lecturer about the expectations for assessments helps and motivates learning.

Recommendation
This practice of clear and timely communications to expectations about assessments will be continued in the future offering of the unit.

Feedback from Unit's survey

Feedback
The laboratory was a challenging but enjoyable learning and assessment activity.

Recommendation
The laboratory is an integral part of the unit learning. Its content and delivery will be continued to be updated and improved.

Feedback from Unit's survey

Feedback
The laboratory video session was incredibly helpful and made what seems like an impossible task for someone who has little experience with the material doable.

Recommendation
A video of the lab will be made available to support students doing the laboratory in the future offering of the unit.

Feedback from Unit's survey

Feedback
The design project was by far the most enjoyable aspect of the unit.

Recommendation
The design project provides an important learning opportunity and assessment task for students doing this unit and therefore it will be maintained and improved.

Feedback from Unit's survey

Feedback
Residential school was replaced with zoom sessions. This had a negative impact on the learning experience and caused difficulties in doing the laboratory and associated assessments.

Recommendation
In Term 1, 2020, the residential school was run due to COVID-19 restrictions. It is acknowledged that the Zoom sessions were interim solutions and could not deliver the same effectiveness and the learning outcomes as a residential school. The residential school will be resumed in future unit's offering when restrictions are lifted.

Feedback from Unit's survey

Feedback
Some aspects of the design project felt like they were outside of the scope of learning and impossible to do even after reviewing the lecture materials over and over again.

Recommendation
The design project is a major assessment and a challenging task. Students are required to integrate and apply the knowledge learned within the unit to conceive the project's solution. Although no additional knowledge outside the unit's materials would be needed, students however require to exercise their problem solving skills and sometimes carry out small research. Guidance and scaffolding toward the project's solution will be provided in the future to assist students with this task.

Feedback from Unit's survey

Feedback
Feedback on the wrong answers in the assessments was often brief, more detailed feedback would be very helpful for learning.

Recommendation
More detailed feedback will be provided for wrong answers especially for cases when learning could be made.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
2. Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
3. Interpret functional requirements, evaluate circuit options and conceive suitable system designs
4. Verify operation of digital systems though software simulations and practical constructions of digital circuits
5. Explain the various integrated circuit technologies and their future development trends
6. Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
7. Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

The Learning Outcomes for this unit are linked with Engineers Australia's Stage 1 Competency Standard for Professional Engineers, Stage 1 Competency Standard for Engineering Technologists, and Stage 1 Competency Standard for Engineering Associates.

Alignment of Learning Outcomes, Assessment and Graduate Attributes

— N/A Level · Introductory Level · Intermediate Level · Graduate Level ◦ Professional Level ◦ Advanced Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Online Test - 15%	•				•		
2 - Practical Assessment - 30%	•	•	•	•		•	•
3 - Project (applied) - 40%		•	•	•		•	•
4 - Online Test - 15%					•		

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication					•	•	•
2 - Problem Solving	•	•	•	•			
3 - Critical Thinking	•	•	•	•	•		
4 - Information Literacy			•		•	•	
5 - Team Work							•

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
6 - Information Technology Competence				•		•	•
7 - Cross Cultural Competence							
8 - Ethical practice							
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Online Test - 15%		•	•			•				
2 - Practical Assessment - 30%	•	•	•		•	•				
3 - Project (applied) - 40%	•	•	•	•		•				
4 - Online Test - 15%		•	•			•				

Textbooks and Resources

Textbooks

ENEE13020

Prescribed

COMPKIT_ENEE13020
Edition: 1 (2021)
CQU-SET
Binding: Other
ENEE13020

Prescribed

DIGITAL FUNDAMENTAL
Eleventh Global Edition (2015)
Authors: Thomas L. Floyd
Pearson
Harlow , Essex , England
ISBN: 9781292075983
Binding: Paperback

Additional Textbook Information
Additional information for the textbook:
There is also an electronic version of the textbook at a reduced price called "Digital Fundamentals Global Edition VitalSource (11e)", ISBN 9781292075990. Please refer to the publisher's webpage for ordering information http://www.pearson.com.au/9781292075990
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Additional information for the lab-kit:
Distance students have the following options for completing the lab component of this unit:
1. Physically attend any of the lab (these are scheduled in blocks) scheduled in any of the campuses (please refer to time table for the dates and campuses)
2. If you can self-supply the equipment required for conducting the labs as listed below, you do not need to purchase TMKIT. You can complete the labs at home without attending the scheduled labs.
You need to purchase TMKIT which has the following items in case you are unable to do 1 or 2 above, please purchase TMKIT (this kit has brand new equipment) or TMKITU (a limited number of TMKITU are available which comprise used equipment on campus before. TMKITU comes with a replacement warranty from school of engineering and technology).
COMPKIT_ENEE13020
Please see additional information on TMKIT or TMKITU (above).
Those who decide to order TMKIT or TMKITU should also order one COMPKIT_ENEE13020, which has all the components required to complete the labs of this unit from home.

View textbooks at the CQUniversity Bookshop

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Microsft Office
- Zoom Conferencing (Webcam and Microphone)
- National Instruments, NI Multisim Education Edition, version 14 or later
- PC with Microsoft Windows as NI Multisim does not run non-windows platform

Referencing Style

All submissions for this unit must use the referencing style: Harvard (author-date)
For further information, see the Assessment Tasks.

Teaching Contacts

Lam Bui Unit Coordinator
l.bui@cqu.edu.au

Schedule

Week 1 - 08 Mar 2021

Module/Topic	Chapter	Events and Submissions/Topic
Overview of teaching arrangement Introductory concepts	Chapter 1 of textbook	None

Week 2 - 15 Mar 2021

Module/Topic	Chapter	Events and Submissions/Topic
Number systems and Logic gates	Chapters 2 and 3 of textbook	None

Week 3 - 22 Mar 2021

Module/Topic	Chapter	Events and Submissions/Topic
Boolean algebra and Logic simplification	Chapter 4 of textbook	None

Week 4 - 29 Mar 2021

Module/Topic	Chapter	Events and Submissions/Topic
Combinational logic analysis	Chapter 5 of textbook	None

Week 5 - 05 Apr 2021

Module/Topic	Chapter	Events and Submissions/Topic
Functions of combinational logic	Chapter 6 of textbook	None

Vacation Week - 12 Apr 2021

Module/Topic	Chapter	Events and Submissions/Topic
No teaching	Not applicable	Online test 1 opened (Friday)

Week 6 - 19 Apr 2021

Module/Topic	Chapter	Events and Submissions/Topic
Latches, flip-flops and timers	Chapter 7 of textbook	None

Week 7 - 26 Apr 2021

Module/Topic	Chapter	Events and Submissions/Topic
Shift registers	Chapter 8 of textbook	None **Online Test 1** Due: Week 7 Monday (26 Apr 2021) 11:59 pm AEST

Week 8 - 03 May 2021

Module/Topic	Chapter	Events and Submissions/Topic
Counters	Chapter 9 of textbook	None

Week 9 - 10 May 2021

Module/Topic	Chapter	Events and Submissions/Topic
Programmable logic	Chapter 10 of textbook	None

Week 10 - 17 May 2021

Module/Topic	Chapter	Events and Submissions/Topic
Data storage	Chapter 11 of textbook	None

Week 11 - 24 May 2021

Module/Topic	Chapter	Events and Submissions/Topic
		None
Signal conversion and processing	Chapter 12 of textbook	**Laboratory Report** Due: Week 11 Monday (24 May 2021) 11:59 pm AEST

Week 12 - 31 May 2021

Module/Topic	Chapter	Events and Submissions/Topic
		Online test 2 opened (Friday)
Integrated circuit technologies	Chapter 15 of textbook	**Design Project** Due: Week 12 Monday (31 May 2021) 11:59 pm AEST

Review/Exam Week - 07 Jun 2021

Module/Topic	Chapter	Events and Submissions/Topic
No teaching	Not applicable	None

Exam Week - 14 Jun 2021

Module/Topic	Chapter	Events and Submissions/Topic
		None
No examination	Not applicable	**Online Test 2** Due: Exam Week Monday (14 June 2021) 11:59 pm AEST

Term Specific Information

There is no residential school for mixed mode students this term, instead mixed mode students are advised to purchase the ENEE13020 lab-kit (see the textbook additional information) and nominate a local CQU campus convenient for them to do the laboratory with on-campus students. Alternatively, mixed mode students can choose to do the laboratory independently at the convenience of their home.

Assessment Tasks

1 Online Test 1

Assessment Type
Online Test

Task Description
Online test 1 is designed to assess student understanding and application of the materials covered between Week 1 and Week 5. Particularly, the test will include questions relating to the topics of:

- Introductory concepts
- Binary arithmetic
- Compliments of binary numbers
- Number systems
- Codes and error correction
- Logic gates and programmable logic
- Boolean operations and algebra
- Standard forms of Boolean expressions
- Karnaugh map and expression minimization
- Combinational logic analysis and circuits
- Waveform operation
- Functions of combinational logic

The test is multiple choice question and timed. Some of the questions may require students to perform a design and calculations to arrive at the correct answer. Please ensure that you read the instructions accompanied the test carefully

and understand them clearly prior commencing the test. The test automatically closes when the test time elapses and therefore it is advisable that you move quickly to the next question if getting stuck. Please be aware that you have only ONE chance to complete the test.

Assessment Due Date
Week 7 Monday (26 Apr 2021) 11:59 pm AEST
The test opens on Friday of Week 5 and closes on Monday of Week 7. It is important to complete the online test within this period since after closing the test cannot be reopened.

Return Date to Students
Week 9 Tuesday (11 May 2021)
Test results are often returned to students within two weeks after the test closes.

Weighting
15%

Assessment Criteria
For each question, student must choose the **most correct** answer. Only the correct answer will result in the award of a full mark. A wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 1 opens on Friday of Week 5 and closes on Monday of Week 7. It is important to complete the online test within this period as after closing the test cannot be reopened.

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

2 Laboratory Report

Assessment Type
Practical Assessment

Task Description
Laboratory comprises of two parts. Part 1 is designed to enhance student practical application of the materials covered between Week 1 and Week 5 inclusively. The laboratory part 1 aims to familiarize students with:

- Multisim as a circuit simulation tool for digital electronics
- Using breadboards as a circuit prototyping platform
- Digital integrated circuit (IC) chips
- Digital logic gates
- Logic expressions and their circuit implementations

Part 2 is designed to enhance student practical application of the materials covered between Week 6 and Week 8 inclusively. The laboratory exercises aim to illustrate

- Multisim as a tool for simulating sophisticated digital electronic circuits
- Operations of basic memory elements: latches and flip-flops
- Operations of a 555 timer
- Operations of shift registers
- Operations of digital counters

Students are required to document the laboratory results, discuss their findings in detailed and answer all questions provided in the laboratory instruction sheet. The lab report must be completed using the provided laboratory template. Simulations of circuits must also be performed using Multisim as instructed in the laboratory instructions.

Assessment Due Date
Week 11 Monday (24 May 2021) 11:59 pm AEST
A complete laboratory submission MUST consist of TWO and only two files: 1) a lab report in pdf format and 2) a single zipped file containing all relevant Multisim files used for the lab report. Laboratory files MUST be submitted electronically via Moodle before the deadline

Return Date to Students
Review/Exam Week Tuesday (8 June 2021)
Marked reports often return to students within two weeks of submission deadline.

Weighting
30%

Minimum mark or grade
50%

Assessment Criteria
The provided laboratory template MUST be used for preparing the laboratory report.

- The details of assessment criteria and mark allocation are given as in the Laboratory instruction sheet.
- The laboratory report must include all information and data to support findings. Discussions and answers of questions must be complete as they will be marked.
- There will be marks allocations for Multisim simulations. No mark is awarded for missing or not-working Multisim files. Please ensure that all relevant Multisim files are submitted as per the submission instructions.
- Data, discussions and answers to questions must be consistent and presented professionally as marks are reserved and awarded for technical rigor and completeness.
- Scanning of hand-written texts or hand-drawn diagrams are acceptable but they must be legible. It is strongly recommended that a suitable drawing software are used to produce a professionally looking report.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete laboratory submission MUST consist of TWO and only two files: 1) a lab report in pdf format and 2) a single zipped file containing all relevant Multisim files used for the lab report. Laboratory files MUST be submitted electronically via Moodle before the deadline

Learning Outcomes Assessed

- Discuss digital number systems, their operations and explain how these systems are used in the processing of digital information
- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Team Work
- Information Technology Competence

3 Design Project

Assessment Type
Project (applied)

Task Description
This project presents an opportunity for students to demonstrate their collective understanding of digital electronics and

apply its principles and methods in the design of practical real-life applications. This project therefore requires students to integrate the learning and the materials covered between Week 1 and Week 8 inclusively. The project requires knowledge of the following topics:

- Fundamental concepts
- Number systems
- Coding, decoding and codes conversions
- Combinational logic analysis
- Functions of combinational logic
- Digital memories and their operations
- Shift registers
- Digital Counters

A detailed description of the project is provided in the project information document and the project reporting template. This project specifically requires students to conceive the system design based on the specified operational requirements of a real life application. The project must be designed in a modular form where students derive the relevant logic expression for each module, implement the modules one by one and demonstrate their correct operation using Multisim simulations. Students also require to integrate the modules together to create a complete working system.
A complete project submission must contain ONLY TWO files: 1) a single project report in a PDF format and 2) a single zipped file containing all relevant and necessary Multisim file implementation of the project that are executable using Multisim. The Multisim implementation of the project will be executed to verify for correct operations during project marking.

Assessment Due Date
Week 12 Monday (31 May 2021) 11:59 pm AEST
A complete submission must contain of TWO only two files: 1) a single report file in pdf format and 2) a single zipped file of all relevant Multisim implementations/simulations of the project. The project files MUST be submitted electronically via Moodle before the deadline

Return Date to Students

Project mark will be withhold until grade certification completed as it is the last assignment of this unit.

Weighting
40%

Minimum mark or grade
50%

Assessment Criteria

- The detailed assessment criteria are provided in the project information document and the project reporting template.
- The project report MUST be completed using the the provided reporting template.
- Students must achieve at least 50% mark for the project to PASS this unit.
- No mark is awarded for parts of report with missing or not working Multisim files. Please also ensure that the submitted Multisim files are executable by the current version of Multisim (version 14).

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
A complete submission MUST and contains ONLY TWO files: 1) a PDF project report and 2) a zipped file containing all relevant Multisim files. The project files MUST be submitted electronically via Moodle before the deadline

Learning Outcomes Assessed

- Analyse the operation of combinational and sequential logic circuits within the discrete and Integrated Circuit (IC) digital electronic devices
- Interpret functional requirements, evaluate circuit options and conceive suitable system designs
- Verify operation of digital systems though software simulations and practical constructions of digital circuits
- Use appropriate electronic engineering terminologies and symbols that conform to Australian Standards to

prepare technical documentations for basic digital system designs and applications
- Work collaboratively and autonomously to solve problems, document and communicate clearly and professionally the approaches used to solve problems.

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Literacy
- Information Technology Competence

4 Online Test 2

Assessment Type
Online Test

Task Description
Online test 2 is designed to assess student understanding and application of the materials covered between Week 9 and Week 12. Particularly, the test will include questions relating to the following topics:

- Programmable logic: architecture, operating modes, programming processes.
- Digital memories: architectures, operations, special types of memory, memory hierarchy
- Conversions between analog and digital signals: principles, methods, Nquist theorem, aliasing, quantisation error
- Electronic integrated technologies: MOSFET versus BJT, operational parameters, and practical considerations

This test comprises of multiple choice questions and will be timed. Some of the questions require students to perform a design and calculations to arrive at the correct answers. Please ensure that you read the instructions accompanied the test carefully and understand them clearly prior commencing the test. The test will automatically end when the test time elapses and therefore it is advisable that you move quickly to the next question if you are getting stuck at the current question. Please be aware that you have only ONE chance to complete the test.

Assessment Due Date
Exam Week Monday (14 June 2021) 11:59 pm AEST
Online test 2 opens on Friday of Week 12 and closes on Monday of Week 14 (Exam Week). It is important to complete the online test within this period as the test cannot be reopened after closing

Return Date to Students

The result of online test 2 will be available within two weeks of the test closing

Weighting
15%

Assessment Criteria
For each question, student must choose the **most correct** answer. Only correct answer will result in the award of a full mark. A wrong choice of answer will result in zero mark.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Online test 2 opens on Friday of Week 12 and closes on Monday of Week 14 (Exam Week). It is important to complete the online test within this period as the test cannot be reopened after closing

Learning Outcomes Assessed

- Explain the various integrated circuit technologies and their future development trends

Graduate Attributes

- Problem Solving
- Critical Thinking
- Information Technology Competence

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the **Student Academic Integrity Policy and Procedure**. This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?
A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?
A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?
For academic advice and guidance, the Academic Learning Centre (ALC) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?

Be Honest
If your assessment task is done by someone else, it would be dishonest of you to claim it as your own

Seek Help
If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)

Produce Original Work
Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem