ENEX13002 *Power Electronics*
Term 2 - 2018

Profile information current as at 22/05/2024 08:45 am

All details in this unit profile for ENEX13002 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

General Information

Overview
This unit is based on your knowledge on electronics you previously studied. In this unit you will learn about power semiconductors such as Diacs, silicon controlled rectifiers (SCR), metal oxide silicon field effect transistors (MOSFET), isolated gate bipolar junction transistors (IGBT), their symbols and theory of operation and limitations. You will also learn to calculate thermal dissipation requirements of power semiconductors and to choose suitable heat sinks. You will be introduced to the concepts of alternating current (AC) to direct current (DC), DC to DC, and DC to AC circuits, pulse width modulation (PWM) control, and chopper circuits. You will also learn about different types of motors and their control including DC motor control, AC motor control and stepper motor control schemes. You will learn to simulate power electronic circuits and develop power electronics solutions industrial problems. Students enrolled in distance mode are required to attend a compulsory Residential School.

Details
Career Level: *Undergraduate*
Unit Level: *Level 3*
Credit Points: *6*
Student Contribution Band: *8*
Fraction of Full-Time Student Load: *0.125*

Pre-requisites or Co-requisites
Prerequisites: ENEX12002 Introductory Electronics OR (ENEE13018 Analogue Electronics and ENEE13020 Digital Electronics) AND (ENEX12001 Electrical Power and Machines OR ENEE12015 Electrical Power Engineering)
Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the Assessment Policy and Procedure (Higher Education Coursework).

Offerings For Term 2 - 2018
- Mackay
- Mixed Mode

Attendance Requirements
All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools
This unit has a Compulsory Residential School for distance mode students and the details are:
Click here to see your Residential School Timetable.

Website
This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

Regional Campuses
Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

Metropolitan Campuses
Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Written Assessment**
Weighting: 15%
2. **Written Assessment**
Weighting: 15%
3. **Practical and Written Assessment**
Weighting: 15%
4. **Practical and Written Assessment**
Weighting: 15%
5. **Examination**
Weighting: 40%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the University's Grades and Results Policy for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the CQUniversity Policy site.
You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the CQUniversity Policy site.

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from Have your say survey

Feedback
The students say unit providing a solid introduction and gave understanding of power electronics.

Recommendation
The existing unit learning material on power electronics will remain the same and further supporting material will be provided as applicable in the future.

Feedback from Have your say survey

Feedback
The students found the tutorial solutions were useful for learning.

Recommendation
Will continue to provide tutorial solutions in the future.

Feedback from Have your say survey

Feedback
Some of the students found the mathematics used in the lectures was hard to understand.

Recommendation
The unit coordinator checked with the mathematics lecturers and found that all the mathematical formulae and methods used in this unit have been covered by the students in the foundation levels. Unfortunately, the time does not permit to teach mathematics within this unit and it is clearly mentioned to the students that they need to go through their Year 1 and 2 mathematics lecture notes. The unit coordinator will develop a list of recommended topics in mathematics of what they have learnt earlier.

Feedback from Have your say survey

Feedback
The Distance students requested tutorial sessions after 5:00pm with Zoom access.

Recommendation
The unit coordinator will try to accommodate this request as much as possible.

Feedback from Have your say survey

Feedback
Students struggled to interpret the assessment criteria.

Recommendation
Assessment criteria will be reviewed and simplified.

Feedback from Self reflection

Feedback
The high level of mathematical nature of the textbook made it harder for some students to understand.

Recommendation
The textbook will be reviewed.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Explain power semiconductors and their principles of operation
2. Analyse and model the operation of alternating current (AC) to direct current (DC), DC to DC, DC to AC power converters and inverters
3. Analyse single phase and three phase rectifier circuits, inverter circuits, and different motor control schemes
4. Compare and select power electronics drive components for a mechatronic system
5. Design variable speed motor controllers for different types of electric motors and evaluate their performances
6. Solve real life problems and communicate professionally using power electronic terminology
7. Work collaboratively and autonomously and communicate professionally in presenting your solutions

Learning outcomes are linked to Engineers Australia Stage 1 Competencies and also discipline capabilities. You can find the mapping for this on the Engineering Undergraduate Course website.

Alignment of Learning Outcomes, Assessment and Graduate Attributes

— N/A Level ◦ Introductory Level • Intermediate Level • Graduate Level ◦ Professional Level ◦ Advanced Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Written Assessment - 15%	•	•	•				
2 - Written Assessment - 15%	•	•	•				
3 - Practical and Written Assessment - 15%	•	•	•	•	•	•	•
4 - Practical and Written Assessment - 15%	•		•	•		•	•
5 - Examination - 40%	•	•	•				

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication	•	•	•	•		•	•
2 - Problem Solving			•		•	•	•
3 - Critical Thinking	•	•	•	•	•	•	
4 - Information Literacy							
5 - Team Work					•		•
6 - Information Technology Competence	•	•	•	•	•	•	

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
7 - Cross Cultural Competence						•	
8 - Ethical practice				•			
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Alignment of Assessment Tasks to Graduate Attributes

Assessment Tasks	Graduate Attributes									
	1	2	3	4	5	6	7	8	9	10
1 - Written Assessment - 15%	•	•	•			•				
2 - Written Assessment - 15%	•	•	•			•				
3 - Practical and Written Assessment - 15%	•	•	•			•		•		
4 - Practical and Written Assessment - 15%	•	•	•		•	•		•		
5 - Examination - 40%	•	•	•			•				

Textbooks and Resources

Textbooks

ENEX13002

Prescribed

Power Electronics Devices, Circuits, and Applications
4th Edition (International) (2014)
Authors: Muhammad H Rashid
Pearson Education Ltd.
Harlaw , Essex , England
ISBN: 978-0-273-76908-8
Binding: Paperback

Additional Textbook Information

View textbooks at the CQUniversity Bookshop

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Access to a document scanner and a software that can create pdf documents.
- A computer with Windows 7 or later with Admin authority to install NI-Multisim software.

Referencing Style

All submissions for this unit must use the referencing style: Harvard (author-date)
For further information, see the Assessment Tasks.

Teaching Contacts

Preethi Preethichandra Unit Coordinator
d.preethichandra@cqu.edu.au

Schedule

Week 1 - 09 Jul 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Introduction to Power Electronics • Power Diodes and LRC Circuits	Chapters 1 & 2	

Week 2 - 16 Jul 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Diode Rectifiers • Power Transistors	Chapters 3 & 4	

Week 3 - 23 Jul 2018

Module/Topic	Chapter	Events and Submissions/Topic
• DC -DC Conversions	Chapter 5	

Week 4 - 30 Jul 2018

Module/Topic	Chapter	Events and Submissions/Topic
• DC -AC Converters	Chapter 6	

Week 5 - 06 Aug 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Resonant Pulse Inverters • Multilevel Inverters	Chapters 7 & 8	**Assignment 1** Due: Week 5 Friday (10 Aug 2018) 11:55 pm AEST

Vacation Week - 13 Aug 2018

Module/Topic	Chapter	Events and Submissions/Topic

Week 6 - 20 Aug 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Thyristors	Chapter 9	

Week 7 - 27 Aug 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Controlled Rectifiers	Chapter 10	

Week 8 - 03 Sep 2018

Module/Topic	Chapter	Events and Submissions/Topic
• AC Voltage Controllers	Chapter 11	

Week 9 - 10 Sep 2018

Module/Topic	Chapter	Events and Submissions/Topic
• DC Drives	Chapter 14	**Desing Task** Due: Week 9 Friday (14 Sept 2018) 11:55 pm AEST

Week 10 - 17 Sep 2018

Module/Topic	Chapter	Events and Submissions/Topic
• AC Drives	Chapter 15	

Week 11 - 24 Sep 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Power Supplies	Chapter 13	

Week 12 - 01 Oct 2018

Module/Topic	Chapter	Events and Submissions/Topic
• Flexible AC Transmission Lines	Chapter 12	**Design and Build Exercise** Due: Week 12 Friday (5 Oct 2018) 11:55 pm AEST **Laboratory experiments** Due: Week 12 Friday (5 Oct 2018) 11:55 pm AEST

Review/Exam Week - 08 Oct 2018

Module/Topic	Chapter	Events and Submissions/Topic

Exam Week - 15 Oct 2018

Module/Topic	Chapter	Events and Submissions/Topic

Term Specific Information

There is a residential school for this unit(compulsory for non MKY students) and check the CQU handbook for correct dates.

Assessment Tasks

1 Assignment 1

Assessment Type
Written Assessment

Task Description
This assignment is based on LRC transient circuits, characteristics of power semiconductors, their applications on AC to DC, DC to DC, and DC to AC power conversions. Further descriptions will be on the moodle site.

Assessment Due Date
Week 5 Friday (10 Aug 2018) 11:55 pm AEST

Return Date to Students
Week 7 Friday (31 Aug 2018)
Marked assignment and a model answer will be provided.

Weighting
15%

Assessment Criteria
Marks will be allocated for the followings:

1. Application of theoretical fundamentals
2. Explanation of reasons to apply specific theory or method to solve a given problem where applicable
3. Correct circuit diagrams/schematics and relevant input/output waveforms
4. Correct mathematical working and correct answer
5. Neatness and format

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Submit the answers as a single pdf file. You are free to scan and embedd clearly hand written answers into the pdf

Learning Outcomes Assessed

- Explain power semiconductors and their principles of operation
- Analyse and model the operation of alternating current (AC) to direct current (DC), DC to DC, DC to AC power converters and inverters
- Analyse single phase and three phase rectifier circuits, inverter circuits, and different motor control schemes

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Technology Competence

2 Desing Task

Assessment Type
Written Assessment

Task Description
This assignment is based on power semiconductor fundamentals and their applications. You will be given a scenario of real world industrial application and the demand criteria to design a power semiconductor based solution for that. The design should be done in NI Multisim and all relavent analysis has to be done in the simulation environment. More details will be available on Moodle site.

Assessment Due Date
Week 9 Friday (14 Sept 2018) 11:55 pm AEST

Return Date to Students
Week 11 Friday (28 Sept 2018)
Marked assignment will be returned with feedback. However there will be no model answer as there is no unique answer for a design problem.

Weighting
15%

Assessment Criteria
Marks will be allocated for the followings:

1. Application of theoretical fundamentals
2. Explanation of reasons to apply specific theory or method to solve a given problem where applicable
3. Correct circuit diagrams/schematics and relevant input/output waveforms
4. Correct mathematical working and working simulation files
5. Neatness and format

Detailed assessment criteria is available in moodle site.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Submit the design report as a single pdf file. All Multisim or LTspice files shold be in a single directory and submit the zip file of that folder as well.

Learning Outcomes Assessed

- Explain power semiconductors and their principles of operation
- Analyse and model the operation of alternating current (AC) to direct current (DC), DC to DC, DC to AC power converters and inverters
- Analyse single phase and three phase rectifier circuits, inverter circuits, and different motor control schemes

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Technology Competence

3 Design and Build Exercise

Assessment Type
Practical and Written Assessment

Task Description
In this assessment you will design two DC-DC power converters for the given requirements. You need to submit your design report Part I before coming to the lab session/ residential school and it will carry 8 out of 15 marks and assessed individualy. In the lab class you will discuss with your group and compare your designs and will select the best design from all group members' individual designs and fabricate that to test. The test will be carried out in a group environment and the Part II of the design report based on the test will be submitted individually. This part carries 7 out of 15 marks allocated for the this assessment item.
In detailed design criteria will be available in Moodle site.

Assessment Due Date
Week 12 Friday (5 Oct 2018) 11:55 pm AEST

Return Date to Students
Exam Week Friday (19 Oct 2018)
Marked design reports will be returned to students. No model answer will be available for designs.

Weighting
15%

Assessment Criteria
Marks will be allocated for the followings:

1. Application of theoretical fundamentals
2. Explanation of reasons to apply specific theory or method to solve a given problem where applicable
3. Correct circuit diagrams/schematics and relevant input/output waveforms
4. Correct mathematical working and working simulation files
5. Contribution in teamwork
6. Neatness and format

Detailed assessment criteria is available in moodle site.

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Submit part I of the design report as a single pdf and submit all Multisim or LTspice files first. Submit part II of the design as design test and evaluation report (as a single pdf file).

Learning Outcomes Assessed

- Explain power semiconductors and their principles of operation
- Analyse and model the operation of alternating current (AC) to direct current (DC), DC to DC, DC to AC power converters and inverters
- Analyse single phase and three phase rectifier circuits, inverter circuits, and different motor control schemes
- Compare and select power electronics drive components for a mechatronic system
- Design variable speed motor controllers for different types of electric motors and evaluate their performances
- Solve real life problems and communicate professionally using power electronic terminology
- Work collaboratively and autonomously and communicate professionally in presenting your solutions

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Information Technology Competence
- Ethical practice

4 Laboratory experiments

Assessment Type
Practical and Written Assessment

Task Description
This assessment item consists of a series of pre-set laboratory experiments on power electronics drives. Detailed explanations of these experiments and how to carry out them are available on Moodle site.

Assessment Due Date
Week 12 Friday (5 Oct 2018) 11:55 pm AEST

Return Date to Students
Exam Week Friday (19 Oct 2018)
Marked lab reports will be returned with feedback. No model answers will be provided.

Weighting
15%

Minimum mark or grade
50% of the allocated marks.

Assessment Criteria
Marks will be allocated to :

1. Following the correct procedures during experimentation
2. Correct results
3. Analysis of results and discussion
4. Conclusions
5. Neatness and format

Referencing Style

- Harvard (author-date)

Submission
Online

Submission Instructions
Submit as a single pdf file

Learning Outcomes Assessed

- Explain power semiconductors and their principles of operation
- Analyse single phase and three phase rectifier circuits, inverter circuits, and different motor control schemes
- Compare and select power electronics drive components for a mechatronic system
- Solve real life problems and communicate professionally using power electronic terminology
- Work collaboratively and autonomously and communicate professionally in presenting your solutions

Graduate Attributes

- Communication
- Problem Solving
- Critical Thinking
- Team Work
- Information Technology Competence
- Ethical practice

Examination

Outline
Complete an invigilated examination.

Date
During the examination period at a CQUniversity examination centre.

Weighting
40%

Length
180 minutes

Minimum mark or grade
50%

Exam Conditions
Open Book.

Materials
Dictionary - non-electronic, concise, direct translation only (dictionary must not contain any notes or comments).
Calculator - all non-communicable calculators, including scientific, programmable and graphics calculators are authorised

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the **Student Academic Integrity Policy and Procedure**. This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?
A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?
A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?
For academic advice and guidance, the Academic Learning Centre (ALC) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?

Be Honest
If your assessment task is done by someone else, it would be dishonest of you to claim it as your own

Seek Help
If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)

Produce Original Work
Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem