



ENEX13002 *Power Electronics*

Term 2 - 2023

Profile information current as at 26/04/2024 07:51 pm

All details in this unit profile for ENEX13002 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

General Information

Overview

In this unit, you will build on your electronics knowledge previously acquired. You will learn more about power semiconductor devices and their modeling, such as diodes, silicon-controlled rectifiers (SCRs), metal oxide silicon field effect transistors (MOSFETs), and isolated gate bipolar junction transistors (IGBTs), including their theory of operation and limitations. You will also learn to calculate thermal dissipation requirements of power semiconductors and to choose suitable heat sinks. You will be introduced to the concepts of alternating current (AC) to direct current (DC), AC to AC, DC to DC, and DC to AC converters. You will analyse circuits and it's waveforms using Fourier analysis. You will also review different types of motors and learn about their drives and control, including DC motor drives and AC motor drives. You will learn to design/develop power electronics solutions and test them by simulation and prototyping in the lab. In this unit, you must complete compulsory practical activities. Refer to the Engineering Undergraduate Course Moodle site for proposed dates.

Details

Career Level: *Undergraduate*

Unit Level: *Level 3*

Credit Points: 6

Student Contribution Band: 8

Fraction of Full-Time Student Load: 0.125

Pre-requisites or Co-requisites

Prerequisites: (ENEX12002 Introductory Electronics OR ENEE13018 Analogue Electronics) AND (ENEX12001 Electrical Power and Machines OR ENEE12015 Electrical Power Engineering) ENEE12015 Electrical Power Engineering may be studied as a co-requisite.

Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the [Assessment Policy and Procedure \(Higher Education Coursework\)](#).

Offerings For Term 2 - 2023

- Bundaberg
- Cairns
- Gladstone
- Mackay
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:

Click here to see your [Residential School Timetable](#).

Website

[This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.](#)

Class and Assessment Overview

Recommended Student Time Commitment

Each 6-credit Undergraduate unit at CQUniversity requires an overall time commitment of an average of 12.5 hours of study per week, making a total of 150 hours for the unit.

Class Timetable

[Regional Campuses](#)

Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

[Metropolitan Campuses](#)

Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

1. **Written Assessment**

Weighting: 20%

2. **Written Assessment**

Weighting: 20%

3. **Practical and Written Assessment**

Weighting: 20%

4. **Online Test**

Weighting: 40%

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the [University's Grades and Results Policy](#) for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the [CQUniversity Policy site](#).

You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure – Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure – International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback – Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the [CQUniversity Policy site](#).

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from Student unit evaluation, email and class.

Feedback

The 'Useful Learning Materials' feedback item scored lower in the unit evaluation. Students have further expressed that the unit workload is high due to excess learning material for this unit.

Recommendation

Review learning material to eliminate peripheral or excess work.

Feedback from Email and class.

Feedback

Self-paced learning is facilitated, seeing much of the unit material is online and available from the start of the semester.

Recommendation

Keep this approach, especially for distance students' sake.

Feedback from Email, class and unit evaluation

Feedback

Students enjoyed the practical approach to the unit and felt that they learned a lot from the assessment tasks.

Recommendation

Keep developing the practical design approach as well as assessment tasks.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Explain the construction of power semiconductor devices, their principle of operation, and their suitability for various switching functions
2. Model power electronic devices for accurate circuit analysis, including their thermal performance
3. Analyse and model the operation of single-phase and three-phase power electronic circuits, including alternating current (AC) to direct current (DC), AC to AC, DC to DC, and DC to AC topologies
4. Compare and select power electronic components, converters, and drives for electromechanical/mechatronic systems
5. Analyse and design variable speed motor drives and controllers for different types of electric motors and evaluate their performances
6. Solve real-life problems and communicate professionally using power electronics terminology
7. Work collaboratively and autonomously and communicate professionally in presenting your solutions.

The Learning Outcomes for this unit are linked with the Engineers Australia Stage 1 Competency Standards for Professional Engineers in the areas of 1. Knowledge and Skill Base, 2. Engineering Application Ability and 3. Professional and Personal Attributes at the following levels:

Intermediate 1.1 Comprehensive, theory-based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline. (LO: 1N 2I 3I 5I) 1.4 Discernment of knowledge development and research directions within the engineering discipline. (LO: 1N 3I 4N 5N 6I) 2.1 Application of established engineering methods to complex engineering problem-solving. (LO: 2I 3I 5I) 2.4 Application of systematic approaches to the conduct and management of engineering projects. (LO: 4N 6I) 3.1 Ethical conduct and professional accountability. (LO: 2I 3I 7N) 3.3 Creative, innovative and pro-active demeanour. (LO: 5I) 3.5 Orderly management of self, and professional conduct. (LO: 6I) 3.6 Effective team membership and team leadership. (LO: 1N 6I 7I)

Advanced 1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline. (LO: 2A 3A 5I 6I) 1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline. (LO: 1N 2A 3A 5I 6I) 1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline. (LO: 3I 4N 6A) 1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline. (LO: 2A 4N 6N) 2.2 Fluent application of engineering techniques, tools and resources. (LO: 2I 3A 6A) 2.3 Application of systematic engineering synthesis and design processes. (LO: 2I 3I 5A) 3.2 Effective oral and written communication in professional and lay domains. (LO: 1N 6A 7I) 3.4 Professional use and management of information. (LO: 1N 4N 6A)

Note: LO refers to the Learning Outcome number(s) which link to the competency and the levels: N - Introductory, I - Intermediate and A - Advanced.

Refer to the Engineering Undergraduate Course Moodle site for further information on the Engineers Australia's Stage 1 Competency Standard for Professional Engineers and course level mapping information <https://moodle.cqu.edu.au/course/view.php?id=1511>



Alignment of Learning Outcomes, Assessment and Graduate Attributes



Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Written Assessment - 20%	•	•		•			•
2 - Written Assessment - 20%			•		•	•	
3 - Practical and Written Assessment - 20%	•			•		•	•
4 - Online Test - 40%		•	•		•		

Alignment of Graduate Attributes to Learning Outcomes

Graduate Attributes	Learning Outcomes						
	1	2	3	4	5	6	7
1 - Communication		•	•	•		•	•
2 - Problem Solving			•		•	•	•
3 - Critical Thinking	•	•	•	•	•	•	
4 - Information Literacy							
5 - Team Work					•		•
6 - Information Technology Competence	•	•	•	•	•	•	
7 - Cross Cultural Competence							
8 - Ethical practice				•		•	•
9 - Social Innovation							
10 - Aboriginal and Torres Strait Islander Cultures							

Textbooks and Resources

Textbooks

ENEX13002

Prescribed

Power Electronics Devices, Circuits, and Applications

4th Edition (International) (2014)

Authors: Muhammad H. Rashid

Pearson Education Ltd.

Harlow , Essex , England

ISBN: 978-0-273-76908-8

Binding: Paperback

Additional Textbook Information

Hardcopy or eBook of the 4th edition would be suitable.

[View textbooks at the CQUniversity Bookshop](#)

IT Resources

You will need access to the following IT resources:

- CQUniversity Student Email
- Internet
- Unit Website (Moodle)
- Multisim 14.0 Education Edition or later (CQU will provide the licence key to install it on student computers).

Referencing Style

All submissions for this unit must use the referencing style: [Harvard \(author-date\)](#)

For further information, see the Assessment Tasks.

Teaching Contacts

Piet Janse Van Rensburg Unit Coordinator

p.jansevanrensburg@cqu.edu.au

Schedule

Week 1 - 10 Jul 2023

Module/Topic	Chapter	Events and Submissions/Topic
<ul style="list-style-type: none">• Introduction to Power Electronics• Power Diodes and LRC Circuits	Chapters 1 & 2	

Week 2 - 17 Jul 2023

Module/Topic	Chapter	Events and Submissions/Topic
<ul style="list-style-type: none">• Diode Rectifiers	Chapter 3	

Week 3 - 24 Jul 2023

Module/Topic	Chapter	Events and Submissions/Topic
<ul style="list-style-type: none">• Power Transistors	Chapter 4	

Week 4 - 31 Jul 2023

Module/Topic	Chapter	Events and Submissions/Topic
<ul style="list-style-type: none">• DC - DC Conversions	Chapter 5	

Week 5 - 07 Aug 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• DC - AC Converters	Chapter 6	Assignment 1 Due: Week 5 Wednesday (9 Aug 2023) 10:00 pm AEST
Vacation Week - 14 Aug 2023		
Module/Topic	Chapter	Events and Submissions/Topic
Week 6 - 21 Aug 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• Multilevel Inverters	Chapter 8	
Week 7 - 28 Aug 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• Resonant Pulse Inverters	Chapter 7	
Week 8 - 04 Sep 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• Thyristors • Controlled Rectifiers	Chapters 9 + 10	
Week 9 - 11 Sep 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• AC Voltage Controllers	Chapter 11	Assignment 2 Due: Week 9 Wednesday (13 Sep 2023) 10:00 pm AEST
Week 10 - 18 Sep 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• DC Drives	Chapter 14	
Week 11 - 25 Sep 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• AC Drives	Chapter 15	
Week 12 - 02 Oct 2023		
Module/Topic	Chapter	Events and Submissions/Topic
• Introduction to Renewable Energy	Chapter 16	Laboratory Panel Experiments - Report is Due: Week 12 Wednesday (4 Oct 2023) 10:00 pm AEST
Review/Exam Week - 09 Oct 2023		
Module/Topic	Chapter	Events and Submissions/Topic
Exam Week - 16 Oct 2023		
Module/Topic	Chapter	Events and Submissions/Topic
		Final Online Test to be conducted during the exam period, date and time to be confirmed by Week 9.

Assessment Tasks

1 Assignment 1

Assessment Type

Written Assessment

Task Description

This **individual** assignment together with feedback, helps to prepare you for the final exam.

The unit content from **Weeks 1 to 4** will be tested in Assignment 1. Questions will be largely analysis based.

Individual work is mandatory - this is a take-home test. None of your steps or solutions may be discussed or divulged to a fellow student.

Please refer to the CQU plagiarism policy - a **signed cover page declaring individual work** is required.

The assignment questions will be released on the unit website at least 2 weeks before the assignment is due to be submitted.

To prevent electronic plagiarism, **typed submissions are not acceptable**. Students should scan clear and legible hand written work for online submission as a **PDF** file.

Assessment Due Date

Please refer to the Schedule section.

Return Date to Students

We strive to return assessments to students within 2 weeks.

Weighting

20%

Assessment Criteria

Marks will be allocated for the followings:

1. Application of theoretical fundamentals.
2. Explanation of reasons to apply specific theory or method to solve a given problem where applicable.
3. Correct circuit diagrams/schematics and relevant input/output waveforms.
4. Correct mathematical working and correct answers.
5. All work and intermediate steps must be shown with justification of steps taken.
6. Assignments must be tidy and legible.

Referencing Style

- [Harvard \(author-date\)](#)

Submission

Online

Submission Instructions

1) Plagiarism statement and 2) complete hand-written assignment scanned in together as a single .pdf file

Learning Outcomes Assessed

- Explain the construction of power semiconductor devices, their principle of operation, and their suitability for various switching functions
- Model power electronic devices for accurate circuit analysis, including their thermal performance
- Compare and select power electronic components, converters, and drives for electromechanical/mechatronic systems
- Work collaboratively and autonomously and communicate professionally in presenting your solutions.

2 Assignment 2

Assessment Type

Written Assessment

Task Description

This **individual** analysis and design based assignment helps to prepare you for the final exam.

The unit content from **Weeks 5 to 9** will be tested in Assignment 2.

Individual work is mandatory - this is a take-home test. None of your steps or solutions may be discussed or divulged to a fellow student.

Please refer to the CQU plagiarism policy - a **signed cover page declaring individual work** is required.

The assignment questions will be released on the unit website at least 2 weeks before the assignment is due to be submitted.

To prevent electronic plagiarism, **typed submissions are not acceptable**. Students should scan clear and legible hand written work for online submission as a **PDF** file.

Assessment Due Date

Please refer to the Schedule section.

Return Date to Students

We strive to return assessments to students within 2 weeks.

Weighting

20%

Assessment Criteria

Marks will be allocated for the followings:

1. Application of theoretical fundamentals.
2. Correct theory or method deployed to analyse and/or design power electronic circuitry where applicable.
3. Correct circuit diagrams/schematics and relevant input/output waveforms.
4. Correct mathematical working and correct answers.
5. All work and intermediate steps must be shown with justification of steps taken.
6. Assignments must be tidy and legible.

Referencing Style

- [Harvard \(author-date\)](#)

Submission

Online

Submission Instructions

1) Plagiarism statement, 2) complete hand-written assignment and 3) screen shot of Multisim circuit and results - all scanned in together as a single .pdf file

Learning Outcomes Assessed

- Analyse and model the operation of single-phase and three-phase power electronic circuits, including alternating current (AC) to direct current (DC), AC to AC, DC to DC, and DC to AC topologies
- Analyse and design variable speed motor drives and controllers for different types of electric motors and evaluate their performances
- Solve real-life problems and communicate professionally using power electronics terminology

3 Laboratory Experiments

Assessment Type

Practical and Written Assessment

Task Description

This assessment item consists of a series of laboratory experiments on plug-and-play power electronic circuits and drives.

Teams of 2 students should be formed, and **only ONE combined report** needs to be submitted by BOTH students. Each student should submit a personal **signed cover page declaring the team work done**, specifying the other team member's name.

Team reports must be **professional and typed**, including references.

Photographic evidence is required to prove that the various circuits were constructed and measurements were obtained - for this reason it is required that a team member's hand or fingers be included in all your photographs as a 'signature'. Laboratory sessions are to be published the unit website.

Laboratories are compulsory and all students must attend and pass all laboratory assessments in order to pass the unit. Detailed explanations of these experiments and how to carry them out will be posted on the unit website at the start of the term.

Assessment Due Date

Return Date to Students

Weighting

20%

Minimum mark or grade

A minimum of 50% must be attained for the Laboratory Exercises report in order to pass the unit.

Assessment Criteria

Laboratory Exercise Reports will be graded using the following criteria:

- Correct description of laboratory concepts and procedures;
- Correct calculations, analysis and thinking;
- Photographic evidence that circuits were constructed by the team;
- Correct measurements, answers and units;
- Photographic and other evidence that correct results / measurements were obtained by the team;
- Discussion and understanding of laboratory results;
- **Team reports** must be **professional and typed**, including references;
- All laboratory exercises must be attempted.

Referencing Style

- [Harvard \(author-date\)](#)

Submission

Online

Submission Instructions

Submit as a single pdf file.

Learning Outcomes Assessed

- Explain the construction of power semiconductor devices, their principle of operation, and their suitability for various switching functions
- Compare and select power electronic components, converters, and drives for electromechanical/mechatronic systems
- Solve real-life problems and communicate professionally using power electronics terminology
- Work collaboratively and autonomously and communicate professionally in presenting your solutions.

4 FINAL ONLINE TEST

Assessment Type

Online Test

Task Description

This final Online Test will be held during the University exam period. The exact date and time will be confirmed by the end of week 9.

The Online Test will be released on the day. 5 Hours will be allowed, but this includes 30 minutes for scanning and uploading.

This assessment will be an 'open resource' test including the internet, but you will be required to sign a declaration of individual work done.

I.e. no forum posts, no contact with fellow students or any person proficient in the field, neither virtual contact via the internet to exchange information etc.

It is strongly advised to take one or more break during the 5-hour period and also to eat and drink something.

Late penalties will be deducted at 20% per hour (or proportional part).

Questions during the 5-hour period will be taken via email and where necessary, responses will be sent out to everyone via Q&A emails.

Assessment Due Date

The Final Online Test takes place during the exam period, exact date to be published on the unit website by week 9.

Return Date to Students

Per CQU policy and because of time pressures before certification of grades, detailed feedback will not be given for the final online test, only a breakdown of marks. General feedback will be released, applicable to the class as a whole.

Weighting

40%

Minimum mark or grade

A minimum of 50% must be attained for the Final Online Test in order to pass the unit.

Assessment Criteria

Marks will be allocated for the followings:

1. Application of theoretical fundamentals.
2. Correct theory or method deployed to analyse and/or design power electronic circuitry where applicable.
3. Correct circuit diagrams/schematics and relevant input/output waveforms.
4. Correct mathematical working and correct answers.

5. All work and intermediate steps must be shown with justification of steps taken.
6. Work must be tidy and legible.

Referencing Style

- [Harvard \(author-date\)](#)

Submission

Online

Submission Instructions

1) Plagiarism statement, 2) Complete hand-written assignment with screen shots of Multisim/Excel results - all scanned in together as a single .pdf file. 3) Multisim/Excel files.

Learning Outcomes Assessed

- Model power electronic devices for accurate circuit analysis, including their thermal performance
- Analyse and model the operation of single-phase and three-phase power electronic circuits, including alternating current (AC) to direct current (DC), AC to AC, DC to DC, and DC to AC topologies
- Analyse and design variable speed motor drives and controllers for different types of electric motors and evaluate their performances

Academic Integrity Statement

As a CQUniversity student you are expected to act honestly in all aspects of your academic work.

Any assessable work undertaken or submitted for review or assessment must be your own work. Assessable work is any type of work you do to meet the assessment requirements in the unit, including draft work submitted for review and feedback and final work to be assessed.

When you use the ideas, words or data of others in your assessment, you must thoroughly and clearly acknowledge the source of this information by using the correct referencing style for your unit. Using others' work without proper acknowledgement may be considered a form of intellectual dishonesty.

Participating honestly, respectfully, responsibly, and fairly in your university study ensures the CQUniversity qualification you earn will be valued as a true indication of your individual academic achievement and will continue to receive the respect and recognition it deserves.

As a student, you are responsible for reading and following CQUniversity's policies, including the [Student Academic Integrity Policy and Procedure](#). This policy sets out CQUniversity's expectations of you to act with integrity, examples of academic integrity breaches to avoid, the processes used to address alleged breaches of academic integrity, and potential penalties.

What is a breach of academic integrity?

A breach of academic integrity includes but is not limited to plagiarism, self-plagiarism, collusion, cheating, contract cheating, and academic misconduct. The Student Academic Integrity Policy and Procedure defines what these terms mean and gives examples.

Why is academic integrity important?

A breach of academic integrity may result in one or more penalties, including suspension or even expulsion from the University. It can also have negative implications for student visas and future enrolment at CQUniversity or elsewhere. Students who engage in contract cheating also risk being blackmailed by contract cheating services.

Where can I get assistance?

For academic advice and guidance, the [Academic Learning Centre \(ALC\)](#) can support you in becoming confident in completing assessments with integrity and of high standard.

What can you do to act with integrity?



Be Honest

If your assessment task is done by someone else, it would be dishonest of you to claim it as your own



Seek Help

If you are not sure about how to cite or reference in essays, reports etc, then seek help from your lecturer, the library or the Academic Learning Centre (ALC)



Produce Original Work

Originality comes from your ability to read widely, think critically, and apply your gained knowledge to address a question or problem