

In Progress

Please note that this Unit Profile is still in progress. The content below is subject to change.



ENEX20001 *Embedded System Design*

Term 3 - 2023

Profile information current as at 05/10/2023 07:13 am

All details in this unit profile for ENEX20001 have been officially approved by CQUniversity and represent a learning partnership between the University and you (our student). The information will not be changed unless absolutely necessary and any change will be clearly indicated by an approved correction included in the profile.

General Information

Overview

This unit will introduce you to microcontroller basics and their real world applications. You will learn about different microcontroller families and their similarities and differences from an application point of view. You will also learn about microcontroller architecture, memory maps, addressing modes, interrupts, timers, counters, and hardware interfacing of a chosen microcontroller. You will learn how to program a microcontroller in a high level language using an integrated development environment. Advanced topics of reading analog inputs, implementation of USART (Universal Synchronous Asynchronous Receiver Transmitter) connections with external world, PWM (Pulse Width Modulation), will also be covered in this unit. After learning the fundamentals of hardware interfacing you will practice them in a laboratory using a microcontroller development system based on this specific microcontroller and finally design and prototype an authentic application of embedded system in your project using the same development system. Online education students are required to attend the residential school.

Details

Career Level: *Postgraduate*

Unit Level: *Level 8*

Credit Points: *12*

Student Contribution Band: *8*

Fraction of Full-Time Student Load: *0.25*

Pre-requisites or Co-requisites

ENEE14006 Embedded Microcontrollers is an Anti-Requisite for this unit.

Important note: Students enrolled in a subsequent unit who failed their pre-requisite unit, should drop the subsequent unit before the census date or within 10 working days of Fail grade notification. Students who do not drop the unit in this timeframe cannot later drop the unit without academic and financial liability. See details in the [Assessment Policy and Procedure \(Higher Education Coursework\)](#).

Offerings For Term 3 - 2023

- Melbourne
- Mixed Mode
- Rockhampton

Attendance Requirements

All on-campus students are expected to attend scheduled classes – in some units, these classes are identified as a mandatory (pass/fail) component and attendance is compulsory. International students, on a student visa, must maintain a full time study load and meet both attendance and academic progress requirements in each study period (satisfactory attendance for International students is defined as maintaining at least an 80% attendance record).

Residential Schools

This unit has a Compulsory Residential School for distance mode students and the details are:

Click here to see your [Residential School Timetable](#).

Website

[This unit has a website, within the Moodle system, which is available two weeks before the start of term. It is important that you visit your Moodle site throughout the term. Please visit Moodle for more information.](#)

Class and Assessment Overview

Recommended Student Time Commitment

Each 12-credit Postgraduate unit at CQUniversity requires an overall time commitment of an average of 25 hours of study per week, making a total of 300 hours for the unit.

Class Timetable

[Regional Campuses](#)

Bundaberg, Cairns, Emerald, Gladstone, Mackay, Rockhampton, Townsville

[Metropolitan Campuses](#)

Adelaide, Brisbane, Melbourne, Perth, Sydney

Assessment Overview

Assessment Grading

This is a graded unit: your overall grade will be calculated from the marks or grades for each assessment task, based on the relative weightings shown in the table above. You must obtain an overall mark for the unit of at least 50%, or an overall grade of 'pass' in order to pass the unit. If any 'pass/fail' tasks are shown in the table above they must also be completed successfully ('pass' grade). You must also meet any minimum mark requirements specified for a particular assessment task, as detailed in the 'assessment task' section (note that in some instances, the minimum mark for a task may be greater than 50%). Consult the [University's Grades and Results Policy](#) for more details of interim results and final grades.

CQUniversity Policies

All University policies are available on the [CQUniversity Policy site](#).

You may wish to view these policies:

- Grades and Results Policy
- Assessment Policy and Procedure (Higher Education Coursework)
- Review of Grade Procedure
- Student Academic Integrity Policy and Procedure
- Monitoring Academic Progress (MAP) Policy and Procedure - Domestic Students
- Monitoring Academic Progress (MAP) Policy and Procedure - International Students
- Student Refund and Credit Balance Policy and Procedure
- Student Feedback - Compliments and Complaints Policy and Procedure
- Information and Communications Technology Acceptable Use Policy and Procedure

This list is not an exhaustive list of all University policies. The full list of University policies are available on the [CQUniversity Policy site](#).

Previous Student Feedback

Feedback, Recommendations and Responses

Every unit is reviewed for enhancement each year. At the most recent review, the following staff and student feedback items were identified and recommendations were made.

Feedback from Unit Coordinator's reflection

Feedback

The use of physical hardware in this unit gave opportunities to apply knowledge into practical problems.

Recommendation

Continue to engage students with practical uses of physical hardware and have exercises and assessments that require students to use physical hardware

Feedback from Unit Coordinator's reflection

Feedback

Further exercises and explanation into some aspects of hardware programming would be useful.

Recommendation

Incorporating and highlighting hardware programming examples in lectures and tutorials and providing more detailed explanation of codes.

Feedback from Unit Survey's Feedback

Feedback

Be more responsive to student emails

Recommendation

Encourage students to exchange questions and ideas on the unit's learning forum as this is beneficial to the entire learning cohort. Educating students that questions that are previously answered in the forum will not be re-answered through personal emails.

Unit Learning Outcomes

On successful completion of this unit, you will be able to:

1. Apply fundamental structured programming knowledge to perform software tasks
2. Program a microcontroller to interface with external devices such as analog and digital sensors, actuators and computers
3. Analyse and design microcontroller based real-time applications using a given industry-standard development system and software tools
4. Prototype an embedded microcontroller system for a real-world application
5. Communicate professionally using relevant technical terminology, symbols, and diagrams and effectively document design and prototyped solutions
6. Work autonomously and as a team member to analyse problems and present solutions.

The Learning Outcomes for this unit are linked with the Engineers Australia Stage 1 Competency Standards for Professional Engineers in the areas of 1. Knowledge and Skill Base, 2. Engineering Application Ability and 3. Professional and Personal Attributes at the following levels:

Introductory

1.2 Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline. (LO: 1N 2N 4N)

Intermediate

1.4 Discernment of knowledge development and research directions within the engineering discipline. (LO: 1I 2I 3I 4I)

3.1 Ethical conduct and professional accountability. (LO: 4I 5I 6I)

3.2 Effective oral and written communication in professional and lay domains. (LO: 5I 6I)

3.3 Creative, innovative and pro-active demeanour. (LO: 1I 2I 3I 4I)

3.4 Professional use and management of information. (LO: 3I 4I 5I 6I)

Advanced

1.1 Comprehensive, theory-based understanding of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline. (LO: 1I 2I 3I 4A)

1.3 In-depth understanding of specialist bodies of knowledge within the engineering discipline. (LO: 1I 2I 3I 4A)

1.5 Knowledge of engineering design practice and contextual factors impacting the engineering discipline. (LO: 1I 2I 3A 4A)

1.6 Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline. (LO: 1I 2I 3I 4A)

2.1 Application of established engineering methods to complex engineering problem solving. (LO: 1I 2I 3I 4A)

2.2 Fluent application of engineering techniques, tools and resources. (LO: 1I 2I 3I 4A)

2.3 Application of systematic engineering synthesis and design processes. (LO: 1I 2I 3A 4A)

2.4 Application of systematic approaches to the conduct and management of engineering projects. (LO: 3A 4A)

3.5 Orderly management of self, and professional conduct. (LO: 4A 5I 6I)

3.6 Effective team membership and team leadership. (LO: 3I 4A 6I)

Note: LO refers to the Learning Outcome number(s) which link to the competency and the levels: N - Introductory, I - Intermediate and A - Advanced.

Refer to the Engineering Postgraduate Units Moodle site for further information on the Engineers Australia's Stage 1 Competency Standard for Professional Engineers and course level mapping information

<https://moodle.cqu.edu.au/course/view.php?id=11382>

Alignment of Learning Outcomes, Assessment and Graduate Attributes



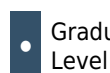
N/A
Level



Introductory
Level



Intermediate
Level



Graduate
Level



Professional
Level



Advanced
Level

Alignment of Assessment Tasks to Learning Outcomes

Assessment Tasks	Learning Outcomes					
	1	2	3	4	5	6

Textbooks and Resources

Information for Textbooks and Resources has not been released yet.

This information will be available on Monday 16 October 2023

Academic Integrity Statement

Information for Academic Integrity Statement has not been released yet.

This unit profile has not yet been finalised.